ACADEMIC REGULATIONS, COURSE STRUCTURE

and

DETAILED SYLLABUS

CHOICE BASED CREDIT SYSTEM

R21

M.Tech – VLSI Design

M.Tech - Regular Two Year Degree Programme
(For batches admitted from the academic year 2021 - 2022)

Holy Mary Institute of Technology & Science
Bogaram (V), Keesara (M), Medchal (Dist) - 501 301

FOREWORD

The autonomy is conferred on Holy Mary Institute of Technology & Science by UGC based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the UGC in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

Holy Mary Institute of Technology & Science is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a two decades in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the college to order to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications, if needed, are to be sought, at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

PRINCIPAL

ACADEMIC REGULATIONS

M. Tech. - Regular Two Year Degree Programme
(For batches admitted from the academic year 2021 - 22)

For pursuing two year post graduate Masters Degree Programme of study in Engineering (M.Tech) offered by Holy Mary Institute of Technology & Science under Autonomous status and herein referred to as HITS (Autonomous):

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2021-22 onwards. Any reference to "Institute" or "College" in these rules and regulations shall stand for Holy Mary Institute of Technology & Science (Autonomous).

All the rules and regulations, specified hereafter shall be read as a whole for the purpose of interpretation as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, Holy Mary Institute of Technology & Science shall be the Chairman, Academic Council.

1. ADMISSION

Admission into first year of two year M. Tech. degree Program of study in Engineering:

Eligibility:

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.
Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt., From time to time.
The medium of instructions for the entire post graduate programme in Engineering & technology will be English only.

2. AWARD OF M. Tech. DEGREE

A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after two academic years of course work, failing which he shall forfeit his seat in M. Tech. programme.

The student shall register for all 68 credits and secure all the 68 credits.
The minimum instruction days in each semester are 90.

3. BRANCH OF STUDY

The following specializations are offered at present for the M. Tech programme of study.

1. Highway Engineering
2. CSE
3. Computer Networks & Information Security
4. Embedded Systems
5. VLSI Design
6. Electrical Power Systems
7. Power Electronics
8. CAD / CAM
9. Machine Design

4. COURSE REGISTRATION

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice / Option for Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work, ensuring 'DATE and TIME Stamping'. The Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during Registration for the Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Course in that Category will be taken into consideration.

4.5 Course Registrations are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new course (subject to offering of such a course), or for another existing course (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5. ATTENDANCE

The programmes are offered on a unit basis with each subject being considered a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the End Semester examination. A student shall not be permitted to appear for the Semester End Examinations (SEE) if his attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below75%) in each semester shall be granted by the College Academic Committee.

5.3 Shortage of Attendance below 65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end semester examination of that subject and their registration shall stand cancelled.

5.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

5.6 A Candidate shall put in a minimum required attendance at least three (3) theory courses in I Year I semester for promoting to I Year II Semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the courses, as per the course structure.

5.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present Semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission in to the same class.

6. EVALUATION

The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for theory and 100 marks for practical's, on the basis of Internal Evaluation and End Semester Examination.

- For the theory courses 70 marks shall be awarded for the performance in the Semester End Examination and 30 marks shall be awarded for Continuous Internal Evaluation (CIE). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other, immediately after the completion of Semester instructions. Each mid-term examination shall be conducted for a total duration of 120 minutes.

Continuous Internal Examination (CIE)

- Subjective Paper shall contain three questions. Question 1 & 2 with internal choice from unit-I, question 3 & 4 with internal choice from unit-II and question no 5 & 6 may be having a, b sub questions with internal choice from first half part of unit-III for CIE-I. For CIE-II 1 & 2 questions from unit-4, questions 3 & 4 from unit-5 and question no 5 & 6 from remaining half part of unit-3. The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus. Question no. 1 to 6 carries 10 Marks.

Semester End Examination (SEE)

- The Semester End Examination will be conducted for 70 marks examination shall be conducted for a total duration of 180 minutes. Question paper consists of Part–A and Part-B with the following.
- Part-A is a compulsory question consisting of 5 questions, one from each unit and carries 4 marks each.
- Part-B to be answered 5 questions carrying 10 marks each. There will be two questions from each unit and only one should be answered.

6.1 For practical courses, 70 marks shall be awarded for performance in the Semester End Examinations and 30 marks shall be awarded for day-to-day performance as Internal Marks.

6.2 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Chief Controller of Examination in one week before for commencement of the lab end examinations.

6.3 There shall be a seminar presentations during II year I semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.4 A candidate shall be deemed to have secured the minimum academic requirement in a Course if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

6.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 6.6) he has to re appear for the Semester End Examination in that course.

6.6 A candidate shall be given one chance to re-register for the courses if the internal marks secured by a candidate is less than 50% and failed in that course for maximum of two courses and should register within four weeks of commencement of the class work. In such a case, the candidate must re-register for the courses and secure the required minimum attendance. The candidate's attendance in the re-registered course(s) shall be calculated separately to decide upon his eligibility for writing the Semester End Examination in those courses. In the event of the student taking another chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stands cancelled.

6.7 In case the candidate secures less than the required attendance in any course, he shall not be permitted to write the Semester End Examination in that course. He shall re-register for the course when next offered.

6.8 Offering one open elective courses in III-Semester along with core and specialized courses as a part of inculcating knowledge to the student.

7. EXAMINATIONS AND ASSESSMENT - THE GRADING SYSTEM

7.1 Marks will be awarded to indicate the performance of each student in each Theory Course, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item6above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	*Letter Grade (UGC Guidelines)*	*Grade Points*
90% and above (≥ 90% , ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥ 80% , < 90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (≥ 70% , < 80%)	A (Very Good)	8
Below 70% but not less than 60% (≥ 60% , < 70%)	B^+ (Good)	7
Below 60% but not less than 50% (≥ 50% , < 60%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	AB	0

7.3 A student obtaining F Grade in any Course shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Courses will remain the same as those he obtained earlier.

7.4 A student not appeared for examination then 'AB' Grade will be allocated in any Course shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Course(s) only for the sake of 'Grade Improvement' or 'SGPA / CGPA Improvement'.

7.7 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject / Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.8 The Student passes the Course only when he **gets GP >=6 (B Grade or above).**

7.9 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course (excluding Mandatory non-credit Courses). Then the corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.10 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP)secured from ALL Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

SGPA = $\{\sum_{i=1}^{N} C_i\, G_i\}$ / $\{\sum_{i=1}^{N} C_i\}$ …. For each Semester,

where 'i' is the Course indicator index (takes into account all Courses in a Semester), 'N' is the no. of Courses 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to that ix Course, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that its Course.

Illustration of Computation of SGPA

Course	Credit	Grade Letter	Grade Point	Credit Point (Credit x Grade)
Course1	3	A	8	3 x 8 = 24
Course2	3	B+	7	4 x 7 = 28
Course3	3	B	6	3 x 6 = 18
Course4	3	O	10	3 x10= 30
Course5	3	C	5	3 x 5 = 15
Course6	3	B	6	4 x 6 = 24

Thus, **SGPA =139/18 =7.72**

7.11 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

CGPA = $\{\sum_{j=1}^{M} C_j\, G_j\}$ / $\{\sum_{j=1}^{M} C_j\}$ … for all S Semesters registered

(i.e., up to and inclusive of S Semesters, S ≥ 2)

where 'M' is the TOTAL no. of Courses (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1st Semester

onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Course indicator index (takes into account all Courses from 1 to S Semesters), C_j is the no. of Credits allotted to the jth Course, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Course. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

For CGPA Computation

Semester 1	Semester 2	Semester 3	Semester 4
Credits : 18 SGPA : 7.72	Credits : 18 SGPA : 7.8	Credits : 12 SGPA : 5.6	Credits : 20 SGPA : 6.0

Thus, **CGPA =** $\dfrac{18 \times 7.72 + 18 \times 7.8 + 12 \times 5.6 + 20 \times 6.0}{68} = 6.86$

7.12 For Calculations listed in Item 7.6 – 7.10, performance in failed Courses (securing F Grade) will also be taken into account, and the Credits of such Courses will also be included in the multiplications and summations.

7.13 No SGPA/CGPA is declared, if a candidate is failed in any one of the courses of a given semester.

7.14 Conversion formula for the conversion of GPA into indicative percentage is

% of marks scored = (final CGPA -0.50) x 10

8. EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of three months between them.

8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 After approval from the PRC, the soft copy of the thesis should be submitted to the College for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 30%, then only thesis will be accepted for submission.

8.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

8.9 For Dissertation Phase-I in II Year I Sem. there is an internal marks of 100, the evaluation should be done by the PRC for 50 marks and Supervisor will evaluate for 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work and Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Phase-I. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

8.10 For Dissertation Phase-II (Viva Voce) in II Year II Sem. There is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The PRC will examine the overall progress of the Project Work and decide the Project is eligible for final submission or not. There is an external marks of 150 and the same evaluated by the External examiner appointed by the Chief Controller of Examinations and he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

8.11 If he fails to fulfill as specified in 8.10, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

8.12 The thesis shall be adjudicated by one examiner selected by the Chief Controller of Examinations. For this, the HOD of the Department shall submit a panel of 3 examiners, eminent in that field, with the help of the guide concerned and Head of the Department.

8.13 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

8.14 If the report of the examiner is favorable, Project dissertation shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

8.15 The Head of the Department shall coordinate and make arrangements for the conduct of Project dissertation.

8.16 For Audit Course (Non-Credit Courses) offered in a Semester, after securing ≥ 65% attendance and has secured not less than 40% marks in the SEE, and a minimum of 50% of marks in the sum Total of the CIE and SEE taken together in such a course, then the student is **PASS** and will be qualified for the award of the degree. No marks or Letter Grade shall be allotted for these courses/activities. However, for non-credit courses '**SATISFACTORY'** or "**UNSATISFACTORY'** shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA.

9. AWARD OF DEGREE AND CLASS

9.1 A Student who registers for all the specified Courses/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of 68 Credits (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 **Award of Class**

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	Grade to be Secured
First Class with Distinction	CGPA ≥ 8.00
First Class	≥ 7.00 to < 8.00 CGPA
Second Class	≥ 6.00 to < 7.00 CGPA

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. WITHOLDING OF RESULTS

If the student has not paid the dues, if any, to the college or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be with held in such cases.

11. TRANSITORY REGULATIONS

11.1 If any candidate is detained due to shortage of attendance in one or more courses, they are eligible for re-registration to maximum of two earlier or equivalent courses at a time as and when offered.

11.2 The candidate who fails in any course will be given two chances to pass the same course; otherwise, he has to identify an equivalent course as per HITS21 Academic Regulations.

12 SUPPLEMENTARY EXAMINATIONS

Supplementary examinations for the odd semester shall be conducted with the regular examinations of even semester and vice versa, for those who appeared and failed or absent in regular examinations. Such candidates writing supplementary examinations may have to write more than one examination.

13. REVALUATION

Students shall be permitted for revaluation after the declaration of end semester examination results within due dates by paying prescribed fee. After revaluation if there is any betterment in the grade, then improved grade will be considered. Otherwise old grade shall be retained.

14. AMENDMENTS TO REGULATIONS

The Academic Council of Holy Mary Institute of Technology & Science reserves the right to revise, amend, or change the regulations, scheme of examinations, and / or syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

15. GENERAL

15.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

15.2 **Credit Point:** It is the product of grade point and number of credits for a course.

15.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”.

15.4 The academic regulation should be read as a whole for the purpose of any interpretation.

15.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

MALPRACTICES RULES - DISCIPLINARY ACTION FOR /IMPROPER CONDUCT IN EXAMINATIONS

S. No	Nature of Malpractices / Improper Conduct	Punishment
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the course of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course.
6	Refuses to obey the orders of the Addl. Controller of examinations / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the addl. Controller of examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the addl. Controller of examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat.

8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that course and all other courses the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the principal for further action to award suitable punishment.	

COURSE STRUCTURE

Dept. of M.Tech – VLSI Design

I Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B1VD101PC	Digital Design and Verification	PC	3	-	-	3	30	70	100
B1VD102PC	Microcontrollers and Programmable Digital Signal Processors	PC	3	-	-	3	30	70	100
B1VD103PC	Low Power VLSI Design	PC	3	-	-	3	30	70	100
	Professional Elective – I	PE	3	-	-	3	30	70	100
	Professional Elective – II	PE	3	-	-	3	30	70	100
B1VD104PC	Digital Design and Verification Lab	PC	-	-	3	1.5	30	70	100
B1VD105PC	Microcontrollers and Programmable Digital Signal Processors Lab	PC	-	-	3	1.5	30	70	100
Total			**15**	**-**	**6**	**18**	**210**	**490**	**700**
Audit Course(Non Credit)									
	Audit Course – I	AC	2	-	-	-	100	-	100

II Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B1VD201PC	Analog and Digital CMOS VLSI Design	PC	3	-	-	3	30	70	100
B1VD202PC	CPLD and FPGA Architectures and Applications	PC	3	-	-	3	30	70	100
B1VD203PC	Advanced Digital System Design	PC	3	-	-	3	30	70	100
	Professional Elective – III	PE	3	-	-	3	30	70	100
	Professional Elective – IV	PE	3	-	-	3	30	70	100
B1VD204PC	Analog and Digital CMOS Lab	PC	-	-	3	1.5	30	70	100
B1VD205PC	VLSI Design and Verification Lab	PC	-	-	3	1.5	30	70	100
Total			**15**	**-**	**6**	**18**	**210**	**490**	**700**
Audit Course(Non Credit)									
	Audit Course – II	AC	2	-	-	-	100	-	100

III Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
	Professional Elective - V	PE	3	-	-	3	30	70	100
	Open Elective	OE	3	-	-	3	30	70	100
B1VD301PC	Technical Seminar	PC	2	-	-	2	100	-	100
B1VD301PW	Dissertation Phase - I	PWC	-	-	16	8	100	-	100
	Total		**8**	**-**	**16**	**16**	**260**	**140**	**400**

IV Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B1VD402PW	Dissertation Phase - II	PWC	-	-	32	16	50	150	200
	Total		**-**	**-**	**32**	**16**	**50**	**150**	**200**

Total Credits = 68

LIST OF PROGRAM ELECTIVE SUBJECTS

PROFESSIONAL ELECTIVES			
PE- I		**PE – II**	
B1VD101PE	Advanced Computer Architecture	B1VD104PE	DSP Architecture
B1VD102PE	Full Custom IC Design	B1VD105PE	IOT and Its Applications
B1VD103PE	Nanomaterials and Nanotechnology	B1VD106PE	Hardware and Software Co-Design
PE - III		**PE – IV**	
B1VD207PE	Algorithms for VLSI Design Automation	B1VD210PE	Device Modeling
B1VD208PE	SOC Design	B1VD211PE	RF IC Architecture
B1VD209PE	VLSI Signal Processing	B1VD212PE	Design for Testability
PE – V			
B1VD313PE	Parallel Processing		
B1VD314PE	Artificial Intelligence and Machine Learning		
B1VD315PE	Memory Technologies		

LIST OF OPEN ELECTIVES SUBJECTS

OPEN ELECTIVES	
B1VD301OE	Scripting Languages
B1VD302OE	Internet of Things
B1VD303OE	Adhoc and Sensor Networks
B1VD304OE	Information Retrieval Systems

LIST OF AUDIT COURSE SUBJECTS

AUDIT COURSE I		AUDIT COURSE II	
B1VD101AC	English for Research Paper Writing	B1VD203AC	Disaster Management
B1VD102AC	Research Methodology and IPR	B1VD204AC	Personality Development through Life Enlightenment Skills

DETAILED SYLLABUS

I-YEAR (I-SEMESTER)

DIGITAL DESIGN AND VERIFICATION

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD101PC **3 0 0 3**

COURSE OBJECTIVES:

1. To familiarize the concepts of verification
2. To understand Data types and OOPs concepts
3. To study and compare the different logic devices

COURSE OUTCOMES: At the end of this course, students will be able to

1. Familiarity of Front end design and verification techniques and create reusable test environments.
2. Verify increasingly complex designs more efficiently and effectively.
3. Design digital circuits with EDA tools like Cadence, Mentor Graphics.

UNIT-I

Revision of Basic Digital Systems: Combinational Circuits, Sequential Circuits, Logic families Synchronous FSM and asynchronous design, Metastability, Clock distribution and issues, basic building blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, Barrel shifter etc.

UNIT-II

Verilog/VHDL Comparisons and Guidelines, Verilog: HDL fundamentals, simulation, and test- bench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS

UNIT-III

System Verilog and Verification: Verification guidelines, Data types, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization, Introduction to basic scripting language: Perl, Tcl/Tk

UNIT-IV

Current Challenges in Physical Design: Roots of challenges, Delays: Wire load models Generic PD flow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop, Process effects: Process Antenna Effect & Electro migration

UNIT-V

Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's, Applications, Programming PLD's, FPGA with technology: Anti-fuse, SRAM, EPROM, MUX, FPGA structures, and ASIC Design Flows, Programmable Interconnections, Coarse grained reconfigurable devices

TEXT BOOKS:

1. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog”, Doone publications,1998.
2. Samir Palnitkar, “Verilog HDL: A guide to Digital Design and Synthesis”, Prentice Hall, 2nd Edition,2003.

REFERENCE BOOKS:

1. Doug Amos, Austin Lesea, Rene Richter, “FPGA based Prototyping Methodology Manual”, Synopsys Press,2011.
2. Christophe Bobda, “Introduction to Reconfigurable Computing, Architectures, Algorithms and Applications”, Springer,2007.
3. Janick Bergeron, “Writing Testbenches: Functional Verification of HDL Models”, Second Edition, Springer,2003.

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD102PC **3 0 0 3**

COURSE OBJECTIVES:

1. To Understand Applications & Programming model of ARM Cortex-M3 processor
2. To implement Priority, Vector Tables, LPC 17xx microcontroller etc.
3. To learn about DSP (P-DSP) Processors, VLIW architecture and TMS320C6000 series

COURSE OUTCOMES: At the end of this course, students will be able to

1. Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
2. Identify and characterize architecture of Programmable DSP Processors
3. Develop small applications by utilizing the ARM processor core and DSP processor based platform.

UNIT-I

Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT-II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT-III

LPC 17XX Microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC,WDT.

UNIT-IV

Harvard architecture, Multi-port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT-V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations

TEXT BOOKS:

1. JosephYiu,“ThedefinitiveguidetoARMCortex-M3”,Elsevier,2nd Edition
2. VenkatramaniB. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH , 2nd Edition

REFERENCE BOOKS:

1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designingand Optimizing”, Morgan Kaufman Publication.
2. Steve furber, “ARM System-on-Chip Architecture”, PearsonEducation
3. Frank Vahid and Tony Givargis, “Embedded System Design”,Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instrumentswww.ti.com

LOW POWER VLSI DESIGN

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD103PC **3 0 0 3**

COURSE OBJECTIVES:

1. To design Low power CMOS designs, for digital circuits.
2. To understand sources of power dissipation
3. To gain knowledge on low power circuit design styles for VLSI circuits.
4. To understand power estimation and optimization methods for VLSI circuits.

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Identify the sources of power dissipation in digital IC systems
2. Understand the impact of low power design through various approaches
3. Characterize and model low voltage and low power multiplier methods
4. Understand various memory technologies.

UNIT – I

Introduction: Basic steps of IC fabrication, PMOS, NMOS, CMOS & BiCMOS. SOI process technologies Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects – Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach–Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures

UNIT – III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low- Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low- Voltage Low-Power Logic Styles.

UNIT – IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT – V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low- Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development ofDRAM.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits – Analysis and Design",TMH, 2011
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

REFERENCE BOOKS:

1. Ming-BO Lin, “Introduction to VLSI Systems: A Logic, Circuit and System Perspective”, CRC Press, 2011
2. Anantha Chandrakasan, “Low Power CMOS Design”, IEEE Press/WileyInternational,1998.
3. Kaushik Roy,Sharat C.Prasad,“LowPowerCMOSVLSICircuitDesign”,JohnWiley&Sons,2000.
4. GaryK.Yeap,“PracticalLowPowerDigitalVLSIDesign”,KluwerAcademicPress,2002.
5. A. Bellamour, M. I. Elamasri, “Low Power CMOS VLSI Circuit Design”, Kluwer Academic Press, 1995.
6. Siva G. Narendran, Anatha Chandrakasan, “Leakage in Nanometer CMOS Technologies” Springer, 2005.

ADVANCED COMPUTER ARCHITECTURE
(Professional Elective – I)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD101PE **3 0 0 3**

COURSE OBJECTIVES:

1. To make students know about the Parallelism concepts in Programming
2. To give the students an elaborate idea about the different memory systems and buses.
3. To introduce the advanced processor architectures to the students

COURSE OUTCOMES: At the end of this course, students will be able to

1. Demonstrate concepts of parallelism in hardware/software.
2. Discuss memory organization and mapping techniques
3. Describe architectural features of advanced processors.
4. Interpret performance of different pipelined processors.

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS

1. John P. Shen and MiikkoH. Lipasti, “Modern Processor Design: Fundamentals of Superscalar Processors”, 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., “Computer Architecture and Parallel Processing”, McGraw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk , “Advanced Computer Architecture - A Design Space Approach”, Pearson Education.

FULL CUSTOM IC DESIGN
(Professional Elective – I)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD102PE **3 0 0 3**

COURSE OBJECTIVES:
1. To understand the fundamentals of layout design and it's significance
2. To Compare the semicustom and full custom layout
3. To acquire knowledge on CAD tools

COURSE OUTCOMES: At the end of this course, students will be able to
1. Explain key features, limitations and topics related to CMOS technology
2. Describe full custom integrated circuit design methodology and issues/constraints related to analogue/digital/mixed signal circuit design
3. Design and assess full custom integrated circuit layout
4. Use a complete tool suite (schematic capture, simulation, layout design, physical verification) covering the full custom design of CMOS integrated circuits.

UNIT - I
Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

UNIT - II
Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals

UNIT - III
Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

UNIT - IV
Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

UNIT - V
Proper layout CAD tools for layout, Planning tools, Layout generation tools, Support tools.

TEXT BOOK:
1. DanClein, "CMOS IC Layout Concepts Methodologies and Tools", Newnes,2000.

REFERENCE BOOK:
1. RayAlanHastings,"TheArtofAnalogLayout",2ndEdition,PrenticeHall, 2006

NANOMATERIALS AND NANOTECHNOLOGY
(Professional Elective – I)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD103PE **3 0 0 3**

COURSE OBJECTIVES:
1. To learn the various nano materials
2. To gain knowledge on SET and Carbon nano tubes in the design of transistors
3. To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Understand the basic science behind the design and fabrication of nano scale systems.
2. Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. Make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.

UNIT - I
Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies.

Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms – Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT - II
Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nanomaterials, Three dimensional nanomaterials. Low-Dimensional Nanomaterials and its Applications, Synthesis, Properties, and Applications of Low-Dimensional Carbon-Related Nanomaterials

UNIT - III
Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics

UNIT - IV
Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT's - Multi-walled nanotubes, Single-walled nanotubes Optical properties of CNT's, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNT's

UNIT - V
Ferroelectric materials, coating, molecular electronics and nanoelectronics, biological and environmental, membrane based application, polymer based application.

TEXT BOOKS
1. Kenneth J. Klabunde and Ryan M. Richards, "Nanoscale Materials in Chemistry", 2 edition, John Wiley and Sons, 2009.
2. I Gusev and A A Rempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1 stIndian edition by Viva Books Pvt. Ltd.2008.
3. B. S. Murty, P. Shankar, BaldevRaj, B. B. Rath, James Murday, "Nanoscience and Nanotechnology", Tata McGraw Hill Education2012.

REFERENCE BOOKS

1. Bharat Bhushan, “Springer Handbook of Nanotechnology”, Springer, 3rd edition, 2010.
2. Kamal K. Kar, “Carbon Nanotubes: Synthesis, Characterization and Applications”, Research Publishing Services; 1 st edition, 2011, ISBN-13:978-9810863975.

DSP ARCHITECTURE
(Professional Elective – II)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD104PE **3 0 0 3**

COURSE OBJECTIVES:

1. To know the various methods for implementation of DSP systems.
2. To understand the various implementations of DSP architectures
3. To gain knowledge on multi-core DSP architectures and programming

COURSE OUTCOMES: At the end of this course, students will be able to

1. Identify and formalize architectural level characterization of P-DSP hardware
2. Ability to design, programming (assembly and C), and testing code using Code Composer Studio environment
3. Deployment of DSP hardware for Control, Audio and Video Signal processing applications
4. Understanding of major areas and challenges in DSP based embedded systems

UNIT-I

Programmable DSP Hardware: Processing Architectures (von Neumann, Harvard), DSP core algorithms (FIR, IIR, Convolution, Correlation, FFT), IEEE standard for Fixed and Floating Point Computations, Special Architectures Modules used in Digital Signal Processors (like MAC unit, Barrel shifters), On-Chip peripherals, DSP benchmarking.

UNIT-II

Structural and Architectural Considerations: Parallelism in DSP processing, Texas Instruments TMS320 Digital Signal Processor Families, Fixed Point TI DSP Processors: TMS320C1X and TMS320C2X Family,TMS320C25 –Internal Architecture, Arithmetic and Logic Unit, Auxiliary Registers, Addressing Modes (Immediate, Direct and Indirect, Bit-reverse Addressing), Basics of TMS320C54x and C55x Families in respect of Architecture improvements and new applications fields, TMS320C5416 DSP Architecture, Memory Map, Interrupt System, Peripheral Devices, Illustrative Examples for assembly coding.

UNIT-III

VLIW Architecture: Current DSP Architectures, GPUs as an alternative to DSP Processors, TMS320C6X Family, Addressing Modes, Replacement of MAC unit by ILP, Detailed study of ISA, Assembly Language Programming, Code Composer Studio, Mixed Cand Assembly Language programming, On-chip peripherals, Simple applications developments as an embedded environment.

UNIT-IV

Multi-Core DSPs: Introduction to Multi-core computing and applicability for DSP hardware, Concept of threads, introduction to P-thread, mutex and similar concepts, heterogeneous and homogenous multi- core systems.

UNIT-V

Shared Memory Parallel Programming: Open MP approach of parallel programming, PRAGMA directives, OpenMP Constructs for work sharing like for loop, sections, TI TMS320C6678 (Eight Core subsystem).

TEXT BOOKS:

1. M. Sasikumar, D. Shikhare, Ravi Prakash, “Introduction to Parallel Processing”, 1st Edition,PHI, 2006.
2. Fayez Gebali, “Algorithms and Parallel Computing”,1st Edition, John Wiley & Sons,2011
3. Rohit Chandra, Ramesh Menon, Leo Dagum, David Kohr, DrorMaydan, Jeff McDonald,“Parallel Programming in OpenMP”, 1st Edition, MorganKaufman,2000

REFERENCE BOOKS:

1. Ann Melnichuk, Long Talk, “Multicore Embedded systems”, 1st Edition, CRC Press, 2010.
2. Wayne Wolf, “High Performance Embedded Computing: Architectures, Applications and Methodologies”, 1st Edition, Morgan Kaufman, 2006.
3. E.S. Gopi, “Algorithmic Collections for Digital Signal Processing Applications Using MATLAB”, 1st Edition, Springer Netherlands, 2007.

IOT AND ITS APPLICATIONS
(Professional Elective – II)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD105PE **3 0 0 3**

COURSE OBJECTIVES:

1. To learn IOT technology, security, standardization.
2. To learn IOT radiation, design principle.
3. To learn about private implementation security issues in platform and design IOT application for industrial use.

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand the concept of IOT and M2M
2. Study IOT architecture and applications in various fields
3. Study the security and privacy issues in IOT.

UNIT-I

IoT & Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.

UNIT-II

M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT-III

IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

UNIT-IV

IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

UNIT-V

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues,

TEXT BOOKS:

1. Vijay Madisetti and ArshdeepBahga, “Internet of Things (A Hands-on-Approach)”, 1st Edition, VPT, 2014.
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1st Edition, Apress Publications,2013.

REFERENCE BOOK:

1. Cuno Pfister, “Getting Started with the Internet of Things”, O Reilly Media,2011.

HARDWARE AND SOFTWARE CO-DESIGN
(Professional Elective – II)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD106PE **3 0 0 3**

COURSE OBJECTIVES:

1. To understand the design of mixed hardware-software systems.
2. To focus on common underlying modeling concepts, the design of hardware-software interfaces, and the trade-offs between hardware and software components.
3. To understand Languages for System – Level Specification and Design

COURSE OUTCOMES:

2. To acquire the knowledge on various models of Co-design.
3. To explore the interrelationship between Hardware and software in a embedded system
4. To acquire the knowledge of firmware development process and tools during Co-design.
5. Understand validation methods and adaptability.

UNIT - I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co- Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, “Hardware / Software Co- Design Principles and Practice”, Wayne Wolf – 2009,Springer
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware / Software Co- Design”, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont,Springer,2010
2. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, 2010, Springer

DIGITAL DESIGN AND VERIFICATION LAB

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD104PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. Understand the concepts of Digital logic
2. Illustrate the concept of combinational and sequential logic
3. Verify and implement the basic digital circuits on FPGA

COURSE OUTCOMES: After completing this course the student will be able to

1. Apply CAD tools for the design of digital circuits.
2. Appreciate the process of synthesizing a given digital circuits.
3. Implement the specified digital circuits using FPGA.

Implementation of the following designs on FPGA using Verilog HDL:

1. 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, Parity generator
2. Code converters
3. D-FF,4-bit Shift registers(SISO, SIPO, PISO, bidirectional), 3-bitSynchronousCounters.
4. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
5. Vending machines -Traffic Light controller, ATM, elevator control.
6. PCI Bus & Arbiter.
7. Single and Dual port SRAM
8. Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD105PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. 1.To Implement the Applications & Programming model of ARM Cortex-M3 processor
2. To implement Priority, Vector Tables, LPC 17xx microcontroller etc.
3. To learn about DSP (P-DSP) Processors, VLIW architecture and TMS320C6000 series

COURSE OUTCOMES: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3.
3. Develop prototype codes using commonly available on and off chip peripherals on DSP development boards.

LIST OF ASSIGNMENTS:

Part A)

Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART cho Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGBLED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B)

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. TodesignandimplementfiltersinCtoenhancethefeaturesofgiveninputsequence/signal

ENGLISH FOR RESEARCH PAPER WRITING
(Audit Course - I)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD101AC **2 0 0 0**

COURSE OBJECTIVES:

1. To improve student writing skills and level of readability
2. To Learn about what to write in each section
3. To develop the student writing skills

COURSE OUTCOMES: At the end of this course students will be able to:

1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title Ensure the good quality of paper at very first- time submission

UNIT-I:

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. DayR(2006)How to Write and Publisha Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.

REFERENCE BOOK:

1. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London,2011

RESEARCH METHODOLOGY AND IPR
(Audit Course - I)

I-M. Tech (I Semester) **L T P C**
Course Code: B1VD102AC **2 0 0 0**

COURSE OBJECTIVES:

1. To understand the research problem
2. To know the literature studies, plagiarism and ethics
3. To get the knowledge about technical writing
4. To analyze the nature of intellectual property rights and new developments

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related in formation
3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.

UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem, Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:

Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT

UNIT-V:

Scope of Patent Rights. Licensing and transfer of technology, Patent information and databases Geographical Indications New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc, Traditional knowledge Case Studies, IPR and IITs

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science &engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd,2007
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand,2008

I-YEAR (II-SEMESTER)

ANALOG AND DIGITAL CMOS VLSI DESIGN

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD201PC **3 0 0 3**

COURSE OBJECTIVES:

1. To understand the fundamentals of MOS technology.
2. To understand the analysis and design of analog and digital CMOS starting from basic building blocks to different implementations of the amplifiers in CMOS technology.
3. To understand CMOS logic styles

COURSE OUTCOMES: At the end of this course, students will be able to

1. Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
2. Connect the individual gates to form the building blocks of a system.
3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

Digital CMOS Design:

UNIT-I

Quality Metrics of a Digital Design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

UNIT-II

Physical Design Flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.
Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT-III

Sequential Logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip- flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit.
Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc

Analog CMOS Design:

UNIT-IV

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT-V

Passive and Active Current Mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

TEXT BOOKS:

1. J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design perspective”, Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.

REFERENCE BOOKS:

1. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, TMH,2007.
2. Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford, 3rd Edition.
3. R J Baker, “CMOS circuit Design, Layout and Simulation”, IEEE Inc., 2008.
4. Kang, S. and Leblebici, Y., “CMOS Digital Integrated Circuits, Analysis and Design”, TMH, 3rd Edition.
5. Pucknell, D.A. and Eshraghian, K., “Basic VLSI Design”, PHI, 3rdEdition

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD202PC **3 0 0 3**

COURSE OBJECTIVES:

1. To understand the features and architectures of industrial CPLDs with different families.
2. To know the programming techniques used in FPGA design methodology.
3. To Design and implement complex real time digital circuits.

COURSE OUTCOMES: At the end of this course, students will be able to

1. Acquire knowledge about various architecture and device technologies of PLDs
2. Understand the FPGA Architecture and programming technologies
3. Design various modules with ACT devices

UNIT-I

IntroductiontoProgrammableLogicDevices: Introduction,SimpleProgrammableLogicDevices–ReadOnly Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, “Field Programmable Gate Array Technology”, Springer International Edition.
2. Charles H.RothJr, Lizy Kurian John, “Digital Systems Design”, Cengage Learning.

REFERENCE BOOKS:

1. Pak K. Chan/Samiha Mourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition.
2. IanGrout,“Digital Systems Design with FPGAs and CPLDs”,Elsevier, Newnes.
3. Wayne Wolf, “Modern Semiconductor Design Series”, Prentice Hall.
4. JohnV.Oldfield,RichardC.Dorf,“FieldProgrammableGateArrays”,WileyIndia

ADVANCED DIGITAL SYSTEM DESIGN

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD203PC **3 0 0 3**

COURSE OBJECTIVES:

1. To study about structural functionality of number system
2. To understand and design combinational logic
3. To understand and design sequential logic
4. To understand subsystem design

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand the numerical information in different forms and Boolean Algebra theorems
2. Apply postulates of Boolean algebra and to minimize combinational functions
3. Design and analyze combinational and sequential circuits

UNIT - I

Processor Arithmetic: Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

UNIT - II

Combinational Circuits: CMOS logic design, Static and dynamic analysis of Combinational circuits, timing hazards. Functional blocks - Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, Carrylook- ahead adder – timing analysis. Combinational multiplier structures.

UNIT - III

Sequential Logic: Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and holdtimes), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and met stability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

UNIT - IV

Subsystem Design using Functional Blocks (1): Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits:

- ALU
- 4-bit combinational multiplier
- Barrel shifter
- Simple fixed point to floating point encoder
- Dual Priority encoder
- Cascading comparators

UNIT - V

Subsystem Design using Functional Blocks (2): Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits:

- Pattern (sequence)detector
- Programmable Up-down counter
- Roundrobinarbiterwith3requesters
- Process Controller
- FIFO

TEXT BOOKS:

1. John F. Wakerly, “Digital Design”, Prentice Hall, 3rd Edition, 2002

*Note1: VHDL and ABEL are not part of this course.
*Note2: SSI & MSI ICs listed in data books are not part of this course.

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(Professional Elective - III)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD207PE **3 0 0 3**

COURSE OBJECTIVES:
1. To understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
2. To discuss the concepts of design optimization algorithms and their application to physical design automation.
3. To understand the concepts of simulation and synthesis in VLSI Design Automation and Formulate CAD design problems using algorithmic methods.

COURSE OUTCOMES: At the end of the course the student will be able to
1. Understand the design methodologies ,automat ion tools to solve various problems
2. Learn the gate and switch level modeling and simulation
3. Analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing

UNIT- I
Preliminaries: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems**.**

UNIT -II
General Purpose Methods for Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT- III
Layout Compaction, Placement, Floor Planning and Routing: Problems, Concepts and Algorithms.
Modelling And Simulation: Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT -IV
Logic Synthesis And Verification: Basic issues and Terminology, Binary-Decision diagrams, Two- Level logic Synthesis.
High-Level Synthesis: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT- V
Physical Design Automation of FPGAs: FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.
Physical Design Automation of MCMs : MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS:
1. S.H. Gerez, “Algorithms for VLSI Design Automation”, 1999, WILEY Student Edition, John Wiley & Sons (Asia) Pvt.Ltd.
2. Naveed Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, 2005, Springer International Edition.

REFERENCE BOOKS:

1. Hill & Peterson, “Computer Aided Logical DesignwithEmphasisonVLSI”,1993, Wiley.
2. Wayne Wolf, “Modern VLSI Design: Systems on silicon”, 2nd ed., 1998, Pearson Education Asia.

SOC DESIGN
(Professional Elective - III)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD208PE **3 0 0 3**

COURSE OBJECTIVES:
1. To learn System on chip fundamentals, their applications.
2. To gain knowledge on SOC design, FPGA.
3. To learn the various computation models of SOCs.

COURSE OUTCOMES: At the end of the course student will be able to
1. Demonstrate the design strategies of CISC,NISC,RISC for SOC
2. Understanding the design and verification of application specific instruction set processors
3. Implement different simulation modes and to minimize the interconnects customization and configuration
4. Implement HDL coding techniques for minimization of power consumption

UNIT-I
ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT-II
NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT-III
Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT-IV
Low Power SoC Design / Digital System Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT-V
Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:
1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press,2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET,2006

REFERENCE BOOKS:

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & DCenter,2000
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann,2008
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley,2011

VLSI SIGNAL PROCESSING
(Professional Elective - III)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD209PE **3 0 0 3**

COURSE OBJECTIVES:
1. To give knowledge about DSP algorithm.
2. To explain about retiming techniques, folding and register minimization path problem.
3. To introduce abut algorithm strength reduction techniques & parallel processing of FIR and IIR filters.
4. To explain about finite word length effects and round off noise computation in DSP.

COURSE OUTCOMES: On successful completion of the module, students will be able to:
1. Ability to modify the existing or new DSP architectures suitable for VLSI
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Ability to implement fast convolution algorithms
4. Low power design aspects of processors for signal processing and wireless applications.

UNIT-I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms
Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power
Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II
Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multi rate systems
Unfolding: Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III
Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV
Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution-Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V
Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches
Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS
1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, WileyInter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall, 1985.

REFERENCE BOOKS
1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing–Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing – MedisettiV. K, IEEE Press (NY),1995

DEVICE MODELLING
(Professional Elective - IV)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD210PE **3 0 0 3**

COURSE OBJECTIVES:

1. To make the student understand how MOSFET and other semiconductor devices are modeled
2. To impart knowledge to simulate MOSFET for various operational requirements.
3. To impart a knowledge on advanced structures of MOSFETs like SOIFET, FinFET etc.

COURSE OUTCOMES: At the end of the course students will be able to

1. Explain the underlying physics and principles of operation of MOS device
2. Derive and compute threshold voltage, and current- voltage characteristics, of a MOS field effect transistor
3. Design MOS signal modelling for various frequencies

UNIT - I

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Mid gap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.

UNIT - II

MOS Capacitor Characteristics and Non Idealities: CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.

UNIT - III

The MOS Transistor: Small signal modeling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

UNIT - IV

The Bipolar Transistor: Eber's-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics.

UNIT - V

FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

TEXT BOOKS:

1. S. M. Sze, "Physics of Semiconductor Devices", 2nd Edition, Wiley Eastern,1981.
2. Y. P. Tsividis, "Operation and Modelling of the MOS Transistor", McGraw-Hill,1987.
3. E. Takeda, "Hot-carrier Effects in MOS Transistors", Academic Press,1995.

REFERENCE BOOK:

1. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer.2009

RF IC ARCHITECTURE
(Professional Elective - IV)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD211PE **3 0 0 3**

COURSE OBJECTIVES:

1. To compare various technique in RF
2. To explore the various performance measures of RF circuits.
3. To acquire knowledge on the design of RF filters, amplifiers and oscillators.
4. To acquire knowledge on design of practical RF circuits

COURSE OUTCOMES: At the end of the course students will be able to

1. Demonstrate in-depth knowledge in Radio Frequency Integrated Circuits.
2. Analyze complex engineering problems critically for conducting research in RF systems.
3. Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
4. Apply appropriate techniques to engineering activities in the field of RFIC Design.

UNIT – I

Introduction to RF and Wireless Technology: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

UNIT – II

Basic Concepts in RF Design: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT – III

Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.

Transceiver Architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT – IV

Amplifiers, Mixers and Oscillators: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT – V

Power Amplifiers: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques

TEXT BOOK:

1. Behzad Razavi, RF Microelectronics Prentice Hall of India,2001.

REFERENCE BOOK:

1. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits**,** Cambridge University Press.

DESIGN FOR TESTABILITY
(Professional Elective - IV)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD212PE **3 0 0 3**

COURSE OBJECTIVES:

1. To know the basics of Faults in digital VLSI circuits
2. To gain knowledge on various testing methods of semiconductor devices.
3. To get an overview on reliability of semiconductors and their testing.
4. To understand testing standards of BIST and Boundary scan.

COURSE OUTCOMES: At the end of the course students will be able to

1. Apply the concept of testing can help them design a better yield in IC design.
2. Learn about different faults in digital circuits and methods of detection and diagnosing
3. Tackle the problems associated with testing of circuits at earlier design levels so as to significantly reduce the testing costs.
4. Identify the design for testability methods for combinational & sequential CMOS circuits.
5. Recognize the BIST techniques for improving testability.

UNIT – I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per- Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design”, Jaico Publishing House.
2. P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

ANALOG AND DIGITAL CMOS LAB

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD204PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. To design Various Amplifier circuits using CMOS Logic.
2. To design Various Complex circuits using Different Logic Styles.
3. To design Layout of Different logic circuits with EDA tools.

COURSE OUTCOMES: At the end of the laboratory work, students will be able to:

1. Design digital and analog Circuit using CMOS.
2. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

LIST OF EXPERIMENTS:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
   a) Plot ID vs. VGS at different drain voltages for NMOS,PMOS.
   b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determineVt.
   c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
   d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS =30mV
      To extract Vth use the following procedure.
      i. Plot gm vs VGS using NGSPICE and obtain peak gm point.
      ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.
      iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.
   Tabulate your result according to technologies and comment on it.
2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
   a) Perform the following
      i. Plot VTC curve for CMOS inverter and thereon plot dVoutvs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)
   c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF,Cload = 4pF,Rload =k)
3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4) Perform the following
   a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and0.13umprocess.
   b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.
      i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.
      ii. Calculate input bias voltage if bias current=50uA.
      iii. Use Ngspice and obtain the bias current. Compare its value with50uA.
      iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).
      v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
      vi. Use Ngspice to determine input voltage range of the amplifier
5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI).Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
      i. Draw the schematic of op-amp macro model.
      ii. Draw the schematic of INA.
      iii. Obtain parameters of the op-amp macro model such that
         a. low-frequency voltage gain =5x104,
         b. unity gain BW (fu) =500KHz,
         c. input capacitance=0.2pF,
         d. output resistance =,
         e. CMRR=120dB
      iv. Draw schematic diagram of CMRR simulation setup.
      v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
      vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
      vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.
6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Micro wind.
   a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
   b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
   c) Useextractednetlistandobtain tPHLtPLHforthemiddleinverterusingEldo.
   d) Use interconnect length obtained and connect the second and third inverter.

Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’

VLSI DESIGN AND VERIFICATION LAB

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD205PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. To design sequential circuits and verify it
2. To design UART module and verify it
3. To design, synthesis and implement in FPGA

COURSE OUTCOMES: At the end of this laboratory students will be able to

1. Design and test FIFO
2. Test and debug the code for multiplexers ,UART module
3. Import the logic modules into FPGA boards

Implementation of the following designs using CAD Tools:

1. Connect two of such FIFOs having different clock rates. Design and test a 2 location 4- bit wide FIFO. Can you explain problems associated with such a setup?

2. Building and testing a parameterized multi-bit adder using control swap (Fredkin) gates as building blocks.

3. Example of some basic circuits, finite state machines (Moore/Mealy).
   Test and debug code for muxes, encoder/decoders, counters, memory access.

4. Serial port design and integration within a system.
   Test and debug the code for a UART module with a FIFO interface. Connect two UART modules and transmit/receive data between them.

5. Introduction to synthesis.
   Run a program to blink an LED on the FPGA. Establish a serial communication between board and computer host.

6. Any of the above designs, implement the physical layout.

DISASTER MANAGEMENT
(Audit Course -II)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD203AC **2 0 0 0**

COURSEOBJECTIVES:

1. To provide basic conceptual understanding of disasters and its relationships with development.
2. To gain understand approaches of Disaster Risk Reduction (DRR)
4. To maintain the relationship between vulnerability, disasters, disaster prevention and risk reduction.

COURSE OUTCOMES: Students will be able to

1. Learn to demonstrate acritical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Developanunderstandingofstandardsofhumanitarianresponseandpractical relevance in specific types of disasters and conflict situations.

UNIT-I:

Introduction:
Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:

Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:

Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation, Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment, Strategies for Survival

UNIT-V:

Disaster Mitigation:
Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India

TEXT BOOKS/ REFERENCE BOOKS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course -II)

I-M. Tech (II Semester) **L T P C**
Course Code: B1VD204PC **2 0 0 0**

PREREQUISITE: None

COURSE OBJECTIVES:
- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

COURSE OUTCOMES: Students will be able to
- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:
Neetisatakam-Holistic development of personality
- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:
Neetisatakam-Holistic development of personality
- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:
Approach to day to day work and duties.
- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:
Statements of basic knowledge.
- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:
- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi

II-YEAR (I-SEMESTER)

PARALLEL PROCESSING
(Professional Elective - V)

II-M. Tech (I Semester) **L T P C**
Course Code: B1VD313PE **3 0 0 3**

COURSE OBJECTIVES:

1. To learn the concept of parallel processing and implementation of pipelining.
2. To introduce upcoming VLIW processor with case study of protocol applications.
3. To introduce multithreaded architecture and discuss various issues & performance protocols.
4. To familiarize with operating systems for multiprocessor system

COURSE OUTCOMES: At the end of this course, students will be able to

1. Identify limitations of different architectures of computer
2. Analysis quantitatively the performance parameters for different architectures
3. Investigate issues related to compilers and instruction set based on type of architectures.
4. Understand processing issues of operating systems for multiprocessor system.

UNIT-I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability, Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT-II

Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT-III

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT-IV

Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

UNIT-V

Operating systems for multiprocessors systems customizing applications on parallel processing platforms

TEXT BOOKS:

1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition
2. Kai Hwang, “Advanced Computer Architecture”, TMH

REFERENCE BOOKS:

1. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.
2. William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition
3. Kai Hwang, ZhiweiXu, “Scalable Parallel Computing”, MGH
4. DavidHarrisandSarahHarris,“DigitalDesignandComputerArchitecture”,MorganKaufmann

ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING
(Professional Elective - V)

II-M. Tech (I Semester) **L T P C**
Course Code: B1VD314PE **3 0 0 3**

COURSE OBJECTIVES:

1. To introduce students to the basic concepts and techniques of Machine Learning.
2. To develop skills of using recent machine learning software for solving practical problems.
3. To gain experience of doing independent study and research.

COURSE OUTCOMES:

1. Apply the basic principles, models, and algorithms of AI in different solutions
2. Recognize, model, and solve problems in the analysis and design of information systems.
3. Analyze the structures and algorithms of a selection of techniques related to searching, reasoning, machine learning, and language processing

UNIT - I

Distance-based methods, Nearest-Neighbours, Decision Trees, Naive Bayes Linear models: Linear Regression, Logistic Regression, Generalized Linear Models Support Vector Machines, Nonlinearity and Kernel Methods Beyond Binary Classification: Multi- class/Structured Outputs, Ranking

UNIT-II

K-means/Kernel K-means Dimensionality Reduction: PCA and kernel PCA Matrix Factorization and Matrix Completion Generative Models (mixture models and latent factor models)

UNIT-III

Evaluating Machine Learning algorithms and Model Selection, Introduction to Statistical Learning Theory, Ensemble Methods (Boosting, Bagging, Random Forests)

UNIT-IV

Artificial Neural Networks. Single layer and Multilayer Feed Forward NN, LMS and Back Propagation Algorithm, Feedback networks and Radial Basis Function Networks

UNIT-V

Fuzzy Logic, Knowledge Representation and Inference Mechanism, Defuzzification Methods Fuzzy Neural Networks and some algorithms to learn the parameters of the network like GA

TEXT BOOKS:

1. Kevin Murphy, Machine Learning: A Probabilistic Perspective, MIT Press,2012
2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning, Springer 2009 (freely available online)

REFERENCE BOOKS:

1. Christopher Bishop, Pattern Recognition and Machine Learning, Springer,2007.
2. J M Zurada , “An Introduction to ANN”,Jaico Publishing House
3. Simon Haykins, “Neural Networks”, Prentice Hall

MEMORY TECHNOLOGIES
(Professional Elective - V)

II-M. Tech (I Semester) **L T P C**
Course Code: B1VD315PE **3 0 0 3**

COURSEOBJECTIVES:

1. To introduce about various type of memory Architectures.
2. To introduce about various performance parameter of memory Architectures.
3. To introduce about various memory packing technologies.
4. To introduce about various 2D & 3D memory Architectures

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Know, how of the state-of-the-art memory chip design
4. Modeling & simulation of memory structure at different technology mode.

UNIT-I

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT-II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers

UNIT-III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT-IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

UNIT-V

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

TEXT BOOKS:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and, Applications” Wiley Inter science
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition

REFERENCE BOOKS:

1. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability, PHI

SCRIPTING LANGUAGES
(Open Elective)

II-M. Tech (I Semester) **L T P C**
Course Code: B1VD301OE **3 0 0 3**

COURSE OBJECTIVES:

1. To develop skills in embedded system programming
2. To provide the ability of identifying the choice of programming language for embedded systems
3. To differentiate interpreted languages from compiled languages.

COURSE OUTCOMES: At the end of this course, students will be able to

1. Write an embedded application of moderate complexity.
2. Develop and analyze algorithms in C++.
3. Differentiate interpreted languages from compiled languages.

UNIT - I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built- in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT - II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT - III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT - IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts- and-bolts' internet programming, Security issues, running untrusted code, The interface.

UNIT - V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.
JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.
Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. David Barron, “The World of Scripting Languages”, Wiley Student Edition, 2010.
2. Brent Welch, Ken Jones and Jeff Hobbs., “Practical Programming in Tcl and Tk” 4th Edition, Prentice Hall
3. Herbert Schildt, “Java the Complete Reference”, 7th Edition, TMH.

REFERENCE BOOKS:

1. Clif Flynt, “Tcl/Tk: A Developer's Guide”, 2003, Morgan Kaufmann Series.
2. John Ousterhout, “Tcland the Tk Toolkit”, 2nd Edition, 2009, Kindel Edition.
3. Wojciech Kocjan and Piotr Beltowski, “Tcl 8.5 Network Programming book”,Packt Publishing.
4. Bert Wheeler, “Tcl/Tk 8.5 Programming Cookbook”, 2011, Packt Publishing Limited.

INTERNET OF THINGS
(Open Elective)

II-M. Tech (I Semester) **L T P C**
Course Code: B1VD302OE **3 0 0 3**

COURSEOBJECTIVES:

1. To learn IOT technology, security, standardization.
2. To learn IOT radiation, design principle.
3. To learn and design IOT application for industrial use.
5. To learn about private implementation security issues in platform

COURSE OBJECTIVES: At the end of the course, students will be able:

1. To introduce the terminology, technology and its applications
2. TointroducetheconceptofM2M (machine to machine) with necessary protocols
3. To introduce the Python Scripting Language which is used in many IoT devices
4. To introduce the Raspberry PI platform, that is widely used in IoT applications

UNIT - I

Introduction to Internet of Things: Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT communication models, Iot Communication APIs IoT enabled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems, IoT Levels and Templates Domain Specific IoTs – Home, City, Environment, Energy, Retail, Logistics, Agriculture, Industry, health and Lifestyle

UNIT - II

IoT and M2M: Software defined networks, network function virtualization, difference between SDN and NFV for IoT Basics of IoT System Management with NETCOZF, YANG- NETCONF, YANG, SNMP NETOPEER

UNIT - III

Introduction to Python: Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages - JSON, XML, HTTPLib, URLLib, SMTPLib

UNIT - IV

IoT Physical Devices and Endpoints: Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, reading input frompins.

UNIT - V

IoT Physical Servers and Cloud Offerings: Introduction to Cloud Storage models and communication APIs Webserver – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API

TEXT BOOKS:

1. Internet of Things - A Hands-on Approach, ArshdeepBahga and Vijay Madisetti, Universities Press, 2015, ISBN:9788173719547
2. Getting Started with Raspberry Pi, Matt Richardson &Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759

REFERENCE BOOKS:

1. VlasiosTsiatsis Stamatis Karnouskos Jan Holler David Boyle Catherine Mulligan, Internet of Things 2ndEdition
2. Jamil Y. Khan, Mehmet R. Yuce, 1st Edition, Internet of Things (IoT) Systems and Applications, Published October 28, 2019 by Jenny Stanford Publishing

AD HOC AND SENSOR NETWORKS
(Open Elective)

II-M. Tech (I Semester) **L T P C**
Course Code: B1VD303OE **3 0 0 3**

COURSEOBJECTIVES:

1. To understand the different issues in Adhoc wireless network.
2. To analyze the design goals of routing protocol for Ad hoc wireless network.
3. To learn about the different routing and transport layer protocols in ad hoc wireless network.
4. To understand QOS and Energy management in Ad hoc wireless network.

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Understand the difference between Adhoc wireless and wireless network.
2. Implement MAC Protocol in Adhoc wireless networks.
3. Design routing protocol in Adhoc wireless networks.
4. Implement QOS and energy management in Adhoc wireless network

UNIT - I

Introduction: Fundamentals of Wireless Communication Technology – The Electromagnetic Spectrum – Radio propagation Mechanisms – Characteristics of the Wireless Channel -mobile ad hoc networks (MANETs) and wireless sensor networks (WSNs): concepts and architectures. Applications of Ad-Hoc and Sensor networks, Design Challenges in Ad hoc and Sensor Networks.

UNIT - II

MAC Protocols For Ad Hoc Wireless Networks: Issues in designing a MAC Protocol- Classification of MAC Protocols- Contention based protocols-Contention based protocols with Reservation Mechanisms-Contention based protocols with Scheduling Mechanisms – Multi channel MAC-IEEE802.11

UNIT - III

Routing Protocols and Transport Layer in Ad Hoc Wireless Networks: Issues in designing a routing and Transport Layer protocol for Ad hoc networks- proactive routing, reactive routing (on-demand), hybrid routing- Classification of Transport Layer solutions-TCP over Ad hoc wireless Networks.

UNIT - IV

Wireless Sensor Networks (WSNS) and MAC Protocols: Single node architecture: hardware and software components of a sensor node – WSN Network architecture: typical network architectures-data relaying and aggregation strategies -MAC layer protocols: self-organizing, Hybrid TDMA/FDMA and CSMA based MAC-IEEE 802.15.4.

UNIT - V

WSN Routing, Localization & QOS: Issues in WSN routing – OLSR- Localization – Indoor and Sensor Network Localization-absolute and relative localization, triangulation-QOS in WSN-Energy Efficient Design-Synchronization-Transport Layer issues

TEXT BOOKS:

1. C. Siva Ram Murthy, and B.S.Manoj,“Ad HocWirelessNetworks: Architectures and Protocols “, Prentice Hall Professional Technical Reference,2008.

REFERENCE BOOKS:

1. Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc & Sensor Networks: Theory and Applications", World Scientific Publishing Company,2006.
2. Feng Zhao and Leonides Guibas, "Wireless Sensor Networks", Elsevier Publication –2002.
3. Holger Karl and Andreas Willig "Protocols and Architectures for Wireless Sensor Networks", Wiley, 2005
4. Kazem Sohraby, Daniel Minoli, &TaiebZnati, "Wireless Sensor Networks-Technology, Protocols, and Applications", John Wiley,2007
5. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

INFORMATION RETRIEVAL SYSTEMS
(Open Elective)

II-M. Tech (I Semester) **L T P C**
Course Code: B1VD304OE **3 0 0 3**

COURSEOBJECTIVES:

1. To present the scientific support in the field of information search and retrieval.
2. To explore the fundamental relationship between information retrieval, hypermedia architecture set
3. To discusses implementation and evaluation issues of new algorithms like clustering, pattern searching,
4. To facilitate a platform to implement comprehensive catalogue of information search tools.

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Usedifferentinformationretrievaltechniquesinvariousapplicationareas
2. Apply IR principles to locate relevant in formation large collections of data
3. Analyzeperformanceofretrievalsystemswhendealingwithunmanageddata sources
4. Implement retrieval systems for web search tasks.

UNIT – I

Boolean retrieval. The term vocabulary and postings lists. Dictionaries and tolerant retrieval. Index construction. Index compression

UNIT – II

Scoring, term weighting, and the vector space model. Computing scores in a complete search system. Evaluation in information retrieval Relevance feedback and query expansion

UNIT – III

XML retrieval. Probabilistic information retrieval. Language models for information retrieval. Text classification. Vector space classification

UNIT – IV

Support vector machines and machine learning on documents, Flat clustering, Hierarchical clustering, Matrix decompositions and latent semantic indexing.

UNIT – V

Web search basics. Web crawling and indexes, Link analysis

TEXT BOOK:

1. Introduction to Information Retrieval , Christopher D. Manning and Prabhakar Raghavan and Hinrich Schütze, Cambridge University Press,2008.

REFERENCE BOOKS:

1. Information Storage and Retrieval Systems: Theory and Implementation, Kowalski, Gerald, Mark T Maybury,Springer.
2. Modern Information Retrieval, Ricardo Baeza-Yates, Pearson Education,2007.
3. Information Retrieval: Algorithms and Heuristics, David A Grossman and Ophir Frieder, 2nd Edition, Springer,2004.
4. Information Retrieval Data Structures and Algorithms, William B Frakes, Ricardo Baeza Yates, Pearson Education,1992.
5. Information Storage &Retieval, Robert Korfhage, John Wiley, &Sons.