ACADEMIC REGULATIONS, COURSE STRUCTURE

and

DETAILED SYLLABUS

CHOICE BASED CREDIT SYSTEM

R21

M.Tech – Embedded Systems

M.Tech - Regular Two Year Degree Programme

(For batches admitted from the academic year 2021 - 2022)

Holy Mary Institute of Technology & Science

Bogaram (V), Keesara (M), Medchal (Dist) - 501 301

FOREWORD

The autonomy is conferred on Holy Mary Institute of Technology & Science by UGC based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the UGC in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

Holy Mary Institute of Technology & Science is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a two decades in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the college to order to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications, if needed, are to be sought, at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

PRINCIPAL

ACADEMIC REGULATIONS

M. Tech. - Regular Two Year Degree Programme
(For batches admitted from the academic year 2021 - 22)

For pursuing two year post graduate Masters Degree Programme of study in Engineering (M.Tech) offered by Holy Mary Institute of Technology & Science under Autonomous status and herein referred to as HITS (Autonomous):

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2021-22 onwards. Any reference to "Institute" or "College" in these rules and regulations shall stand for Holy Mary Institute of Technology & Science (Autonomous).

All the rules and regulations, specified hereafter shall be read as a whole for the purpose of interpretation as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, Holy Mary Institute of Technology & Science shall be the Chairman, Academic Council.

1. ADMISSION

Admission into first year of two year M. Tech. degree Program of study in Engineering:

Eligibility:

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt., From time to time.

The medium of instructions for the entire post graduate programme in Engineering & technology will be English only.

2. AWARD OF M. Tech. DEGREE

A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after two academic years of course work, failing which he shall forfeit his seat in M. Tech. programme.

The student shall register for all 68 credits and secure all the 68 credits.

The minimum instruction days in each semester are 90.

3. BRANCH OF STUDY

The following specializations are offered at present for the M. Tech programme of study.

1. Highway Engineering
2. CSE
3. Computer Networks & Information Security
4. Embedded Systems
5. VLSI Design
6. Electrical Power Systems
7. Power Electronics
8. CAD / CAM
9. Machine Design

4. COURSE REGISTRATION

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice / Option for Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work, ensuring 'DATE and TIME Stamping'. The Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during Registration for the Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Course in that Category will be taken into consideration.

4.5 Course Registrations are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new course (subject to offering of such a course), or for another existing course (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5. ATTENDANCE

The programmes are offered on a unit basis with each subject being considered a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the End Semester examination. A student shall not be permitted to appear for the Semester End Examinations (SEE) if his attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below75%) in each semester shall be granted by the College Academic Committee.

5.3 Shortage of Attendance below 65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end semester examination of that subject and their registration shall stand cancelled.

5.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

5.6 A Candidate shall put in a minimum required attendance at least three (3) theory courses in I Year I semester for promoting to I Year II Semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the courses, as per the course structure.

5.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present Semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission in to the same class.

6. EVALUATION

The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for theory and 100 marks for practical's, on the basis of Internal Evaluation and End Semester Examination.

- For the theory courses 70 marks shall be awarded for the performance in the Semester End Examination and 30 marks shall be awarded for Continuous Internal Evaluation (CIE). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other, immediately after the completion of Semester instructions. Each mid-term examination shall be conducted for a total duration of 120 minutes.

Continuous Internal Examination (CIE)

- Subjective Paper shall contain three questions. Question 1 & 2 with internal choice from unit-I, question 3 & 4 with internal choice from unit-II and question no 5 & 6 may be having a, b sub questions with internal choice from first half part of unit-III for CIE-I. For CIE-II 1 & 2 questions from unit-4, questions 3 & 4 from unit-5 and question no 5 & 6 from remaining half part of unit-3. The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus. Question no. 1 to 6 carries 10 Marks.

Semester End Examination (SEE)

- The Semester End Examination will be conducted for 70 marks examination shall be conducted for a total duration of 180 minutes. Question paper consists of Part–A and Part-B with the following.
- Part-A is a compulsory question consisting of 5 questions, one from each unit and carries 4 marks each.
- Part-B to be answered 5 questions carrying 10 marks each. There will be two questions from each unit and only one should be answered.

6.1 For practical courses, 70 marks shall be awarded for performance in the Semester End Examinations and 30 marks shall be awarded for day-to-day performance as Internal Marks.

6.2 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Chief Controller of Examination in one week before for commencement of the lab end examinations.

6.3 There shall be a seminar presentations during II year I semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.4 A candidate shall be deemed to have secured the minimum academic requirement in a Course if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

6.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 6.6) he has to re appear for the Semester End Examination in that course.

6.6 A candidate shall be given one chance to re-register for the courses if the internal marks secured by a candidate is less than 50% and failed in that course for maximum of two courses and should register within four weeks of commencement of the class work. In such a case, the candidate must re-register for the courses and secure the required minimum attendance. The candidate's attendance in the re-registered course(s) shall be calculated separately to decide upon his eligibility for writing the Semester End Examination in those courses. In the event of the student taking another chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stands cancelled.

6.7 In case the candidate secures less than the required attendance in any course, he shall not be permitted to write the Semester End Examination in that course. He shall re-register for the course when next offered.

6.8 Offering one open elective courses in III-Semester along with core and specialized courses as a part of inculcating knowledge to the student.

7. EXAMINATIONS AND ASSESSMENT - THE GRADING SYSTEM

7.1 Marks will be awarded to indicate the performance of each student in each Theory Course, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item6above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	*Letter Grade (UGC Guidelines)*	*Grade Points*
90% and above (≥ 90% , ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥ 80% , < 90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (≥ 70% , < 80%)	A (Very Good)	8
Below 70% but not less than 60% (≥ 60% , < 70%)	B^+ (Good)	7
Below 60% but not less than 50% (≥ 50% , < 60%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	AB	0

7.3 A student obtaining F Grade in any Course shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Courses will remain the same as those he obtained earlier.

7.4 A student not appeared for examination then 'AB' Grade will be allocated in any Course shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

7.6 In general, a student shall not be permitted to repeat any Course(s) only for the sake of 'Grade Improvement' or 'SGPA / CGPA Improvement'.

7.7 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject / Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.8 The Student passes the Course only when he **gets GP >=6 (B Grade or above).**

7.9 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course (excluding Mandatory non-credit Courses). Then the corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

7.10 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP)secured from ALL Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

SGPA = $\{\sum_{i=1}^{N} C_i G_i\} / \{\sum_{i=1}^{N} C_i\}$ …. For each Semester,

where 'i' is the Course indicator index (takes into account all Courses in a Semester), 'N' is the no. of Courses 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to that ix Course, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that its Course.

Illustration of Computation of SGPA

Course	Credit	Grade Letter	Grade Point	Credit Point (Credit x Grade)
Course1	3	A	8	3 x 8 = 24
Course2	3	B+	7	4 x 7 = 28
Course3	3	B	6	3 x 6 = 18
Course4	3	O	10	3 x10= 30
Course5	3	C	5	3 x 5 = 15
Course6	3	B	6	4 x 6 = 24

Thus, **SGPA =139/18 =7.72**

7.11 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

CGPA = { $\sum_{j=1}^{M} C_j G_j$ } / { $\sum_{j=1}^{M} C_j$ } … for all S Semesters registered

(i.e., up to and inclusive of S Semesters, S ≥ 2)

where 'M' is the TOTAL no. of Courses (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Course indicator index (takes into account all Courses from 1 to S Semesters), C_j is the no. of Credits allotted to the jth Course, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Course. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

For CGPA Computation

Semester 1	Semester 2	Semester 3	Semester 4
Credits : 18 SGPA : 7.72	Credits : 18 SGPA : 7.8	Credits : 12 SGPA : 5.6	Credits : 20 SGPA : 6.0

Thus, **CGPA =** $\dfrac{18 \times 7.72 + 18 \times 7.8 + 12 \times 5.6 + 20 \times 6.0}{68} = 6.86$

7.12 For Calculations listed in Item 7.6 – 7.10, performance in failed Courses (securing F Grade) will also be taken into account, and the Credits of such Courses will also be included in the multiplications and summations.

7.13 No SGPA/CGPA is declared, if a candidate is failed in any one of the courses of a given semester.

7.14 Conversion formula for the conversion of GPA into indicative percentage is

% of marks scored = (final CGPA -0.50) x 10

8. EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of three months between them.

8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 After approval from the PRC, the soft copy of the thesis should be submitted to the College for ANTI-PLAGIARISM for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than 30%, then only thesis will be accepted for submission.

8.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

8.9 For Dissertation Phase-I in II Year I Sem. there is an internal marks of 100, the evaluation should be done by the PRC for 50 marks and Supervisor will evaluate for 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work and Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Phase-I. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

8.10 For Dissertation Phase-II (Viva Voce) in II Year II Sem. There is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The PRC will examine the overall progress of the Project Work and decide the Project is eligible for final submission or not. There is an external marks of 150 and the same evaluated by the External examiner appointed by the Chief Controller of Examinations and he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

8.11 If he fails to fulfill as specified in 8.10, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

8.12 The thesis shall be adjudicated by one examiner selected by the Chief Controller of Examinations. For this, the HOD of the Department shall submit a panel of 3 examiners, eminent in that field, with the help of the guide concerned and Head of the Department.

8.13 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

8.14 If the report of the examiner is favorable, Project dissertation shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

8.15 The Head of the Department shall coordinate and make arrangements for the conduct of Project dissertation.

8.16 For Audit Course (Non-Credit Courses) offered in a Semester, after securing ≥ 65% attendance and has secured not less than 40% marks in the SEE, and a minimum of 50% of marks in the sum Total of the CIE and SEE taken together in such a course, then the student is **PASS** and will be qualified for the award of the degree. No marks or Letter Grade shall be allotted for these courses/activities. However, for non-credit courses '**SATISFACTORY'** or "**UNSATISFACTORY'** shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA.

9. AWARD OF DEGREE AND CLASS

9.1 A Student who registers for all the specified Courses/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of 68 Credits (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 **Award of Class**

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	Grade to be Secured
First Class with Distinction	CGPA ≥ 8.00
First Class	≥ 7.00 to < 8.00 CGPA
Second Class	≥ 6.00 to < 7.00 CGPA

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10. WITHOLDING OF RESULTS

If the student has not paid the dues, if any, to the college or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be with held in such cases.

11. TRANSITORY REGULATIONS

11.1 If any candidate is detained due to shortage of attendance in one or more courses, they are eligible for re-registration to maximum of two earlier or equivalent courses at a time as and when offered.

11.2 The candidate who fails in any course will be given two chances to pass the same course; otherwise, he has to identify an equivalent course as per HITS21 Academic Regulations.

12 SUPPLEMENTARY EXAMINATIONS

Supplementary examinations for the odd semester shall be conducted with the regular examinations of even semester and vice versa, for those who appeared and failed or absent in regular examinations. Such candidates writing supplementary examinations may have to write more than one examination.

13. REVALUATION

Students shall be permitted for revaluation after the declaration of end semester examination results within due dates by paying prescribed fee. After revaluation if there is any betterment in the grade, then improved grade will be considered. Otherwise old grade shall be retained.

14. AMENDMENTS TO REGULATIONS

The Academic Council of Holy Mary Institute of Technology & Science reserves the right to revise, amend, or change the regulations, scheme of examinations, and / or syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

15. GENERAL

15.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

15.2 **Credit Point:** It is the product of grade point and number of credits for a course.

15.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”.

15.4 The academic regulation should be read as a whole for the purpose of any interpretation.

15.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

MALPRACTICES RULES - DISCIPLINARY ACTION FOR /IMPROPER CONDUCT IN EXAMINATIONS

S. No	Nature of Malpractices / Improper Conduct	Punishment
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the course of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course.
6	Refuses to obey the orders of the Addl. Controller of examinations / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the addl. Controller of examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the addl. Controller of examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and

		all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that course and all other courses the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the principal for further action to award suitable punishment.	

COURSE STRUCTURE

M.Tech – Embedded Systems

I Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B1ES101PC	System Design with Embedded Linux	PC	3	-	-	3	30	70	100
B1ES102PC	Microcontrollers & Programmable Digital Signal Processors	PC	3	-	-	3	30	70	100
B1ES103PC	Hardware Software Co-Design	PC	3	-	-	3	30	70	100
	Professional Elective - I	PE	3	-	-	3	30	70	100
	Professional Elective - II	PE	3	-	-	3	30	70	100
B1ES104PC	System Design with Embedded Linux Lab	PC	-	-	3	1.5	30	70	100
B1ES105PC	Microcontrollers & Programmable Digital Signal Processors Lab	PC	-	-	3	1.5	30	70	100
	Total		**15**	**-**	**6**	**18**	**210**	**490**	**700**
Audit Course(Non Credit)									
	Audit Course – I	AC	2	-	-	-	100	-	100

II Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B1ES201PC	RTL Simulation and Synthesis with PLDs	PC	3	-	-	3	30	70	100
B1ES202PC	Advanced Digital Signal Processing	PC	3	-	-	3	30	70	100
B1ES203PC	Embedded Computing	PC	3	-	-	3	30	70	100
	Professional Elective – III	PE	3	-	-	3	30	70	100
	Professional Elective – IV	PE	3	-	-	3	30	70	100
B1ES204PC	Advanced Digital Signal Processing Lab	PC	-	-	3	1.5	30	70	100
B1ES205PC	RTL Simulation and Synthesis with PLDs Lab	PC	-	-	3	1.5	30	70	100
	Total		**15**	**-**	**6**	**18**	**210**	**490**	**700**
Audit Course(Non Credit)									
	Audit Course – II	AC	2	-	-	-	100	-	100

III Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
	Professional Elective - V	PE	3	-	-	3	30	70	100
	Open Elective	OE	3	-	-	3	30	70	100
B1ES301PC	Technical Seminar	PC	2	-	-	2	100	-	100
B1ES301PW	Dissertation Phase - I	PWC	-	-	16	8	100	-	100
	Total		**8**	**-**	**16**	**16**	**260**	**140**	**400**

IV Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B1ES402PW	Dissertation Phase - II	PWC	-	-	32	16	50	150	200
	TOTAL		**-**	**-**	**32**	**16**	**50**	**150**	**200**

Total Credits =68

PROFESSIONAL ELECTIVES			
PE- I		PE – II	
B1ES101PE	Programming Languages for Embedded Software	B1ES104PE	Communications Buses & Interfaces
B1ES102PE	Artificial Intelligence & Machine Leaning	B1ES105PE	Parallel Processing
B1ES103PE	Computer Vision	B1ES106PE	Advanced Computer Architecture
PE - III		PE – IV	
B1ES207PE	IOT and Its Applications	B1ES210PE	Artificial Neural Networks
B1ES208PE	VLSI Signal Processing	B1ES211PE	Network Security and Cryptography
B1ES209PE	SOC Architecture	B1ES212PE	Physical Design Automation
PE – V			
B1ES313PE	Scripting Languages		
B1ES314PE	Memory Technologies		
B1ES315PE	Wireless Sensor Networks		

OPEN ELECTIVES	
B1ES301OE	Artificial Neural Networks
B1ES302OE	Internet of Things
B1ES303OE	Adhoc & Sensor Networks
B1ES304OE	Information Retrieval Systems

AUDIT COURSE I		AUDIT COURSE II	
B1ES101AC	English for Research Paper Writing	B1ES203AC	Disaster Management
B1ES102AC	Research Methodology and IPR	B1ES204AC	Personality Development through Life Enlightenment Skills

DETAILED SYLLABUS

I-YEAR (I-SEMESTER)

SYSTEM DESIGN WITH EMBEDDED LINUX

I-M. Tech I Semester **L T P C**
Course Code: B1ES101PC **3 0 0 3**

COURSE OBJECTIVES:

1. To understand and make effective use of Linux utilities and Shell scripting language (bash) to solve Problems.
2. To implement in C some standard Linux utilities such as ls, mv, cp etc. using system calls.
3. To develop the skills necessary for systems programming including file system programming, process and signal management, and inter process communication

COURSE OUTCOMES: At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Understand and create Linux BSP for a hardware platform

UNIT-I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling.
Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross tool chains

UNIT-II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT-III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules
Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules

UNIT-IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT-V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds “Mastering Embedded Linux Programming” - Second Edition, PACKTPublications Limited.
2. Karim Yaghmour, “Building Imbedded Linux Systems”, O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design andDevelopment”, Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real World Approach”, PrenticeHall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

I-M. Tech I Semester **L T P C**
Course Code: B1ES102PC **3 0 0 3**

COURSE OBJECTIVES:

1. To Understand Applications & Programming model of ARM Cortex-M3 processor
2. To implement Priority, Vector Tables, LPC 17xx microcontroller etc.
3. To learn about DSP (P-DSP) Processors, VLIW architecture and TMS320C6000 series

COURSE OUTCOMES: At the end of this course, students will be able to

1. Compare and select ARM processor core based SoC with several features/peripherals basedon requirements of embedded applications.
2. Identify and characterize architecture of Programmable DSP Processors
3. Develop small applications by utilizing the ARM processor core and DSP processor based platform.

UNIT-I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT-II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT-III

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT-IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architecturalstructure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT-V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations

TEXT BOOKS:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH , 2nd Edition

REFERENCE BOOKS:

1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designingand Optimizing”, Morgan Kaufman Publication.
2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
3. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

HARDWARE SOFTWARE CO-DESIGN

	L	T	P	C
I-M. Tech I Semester				
Course Code: B1ES103PC	**3**	**0**	**0**	**3**

COURSE OBJECTIVES:

1. To understand the design of mixed hardware-software systems.
2. To focus on common underlying modeling concepts, the design of hardware-software interfaces, and the trade-of between hardware and software components.
3. To understand Languages for System – Level Specification and Design

COURSE OUTCOMES: At the end of this course, students will be able to

1. Acquire the knowledge on various models
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools
4. Understand validation methods and adaptability.

UNIT – I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis

UNIT – II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT – IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT – V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, “Hardware / Software Co- Design Principles and Practice”, Wayne Wolf –2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware / Software Co- Design”, 2002, Kluwer Academic Publishers

REFERENCE BOOK:

1. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, 2010,Springer

PROGRAMMING LANGUAGE FOR EMBEDDED SOFTWARE
(Professional Elective-1)

I-M. Tech I Semester | **L T P C**
Course Code: B1ES101PE | **3 0 0 3**

COURSE OBJECTIVES:
1. To develop skills in embedded system programming
2. To provide the ability of identifying the choice of programming language for embedded systems
3. To differentiate interpreted languages from compiled languages.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Write an embedded C application of moderate complexity.
2. Develop and analyze algorithms in C++.
3. Differentiate interpreted languages from compiled languages.

UNIT – I
Embedded 'C' Programming
- Bitwise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, Code optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT – II
CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT – III
Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

UNIT – IV
Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch-throw, MultipleExceptions.

UNIT – V
Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, TiedVariables, Inter process Communication Threads, Compilation & Line Interfacing.

TEXT BOOKS:
1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011

REFERENCE BOOKS:
1. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey &Sons, 2005

ARTIFICIAL INTELLIGENCE & MACHINE LEARNING
(Professional Elective-1)

I-M. Tech I Semester **L T P C**
Course Code: B1ES102PE **3 0 0 3**

COURSE OBJECTIVES:

1. To introduce students to the basic concepts and techniques of Machine Learning.
2. To develop skills of using recent machine learning software for solving practical problems.
3. To gain experience of doing independent study and research.

COURSE OUTCOMES: At the end of this course, students will be able to

1. Apply the basic principles, models, and algorithms of AI in different solutions
2. Recognize, model, and solve problems in the analysis and design of information systems.
3. Analyze the structures and algorithms of a selection of techniques related to searching, reasoning, machine learning, and language processing.

UNIT – I

Supervised Learning (Regression/Classification)

Basic methods: Distance-based methods, Nearest-Neighbors, Decision Trees, Naive Bayes Linear models: Linear Regression, Logistic Regression, Generalized Linear Models Support Vector Machines, Nonlinearity and Kernel Methods

Beyond Binary Classification: Multi-class/Structured Outputs, Ranking

UNIT – II

Unsupervised Learning Clustering: K-means/Kernel K-means Dimensionality Reduction: PCA and kernel PCAMatrix Factorization and Matrix Completion

Generative Models (mixture models and latent factor models)

UNIT – III

Evaluating Machine Learning algorithms and Model Selection: Introduction to Statistical Learning Theory, Ensemble Methods (Boosting, Bagging, Random Forests)

UNIT – IV

Biological foundations to intelligent Systems: Artificial Neural Networks.

Single layer and Multilayer Feed Forward NN, LMS and Back Propagation. Algorithm, Feedback networks and Radial Basis Function Networks

UNIT – V

Fuzzy Logic, Knowledge Representation and Inference Mechanism, Defuzzification Methods FuzzyNeural Networks and some algorithms to learn the parameters of the network like GA

TEXT BOOKS:

1. Kevin Murphy, Machine Learning: A Probabilistic Perspective, MIT Press, 2012
2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning,Springer 2009 (freely available online)

REFERENCE BOOKS:

1. Christopher Bishop, Pattern Recognition and Machine Learning, Springer, 2007.
2. J M Zurada , “An Introduction to ANN”,Jaico Publishing House
3. Simon Haykins, “Neural Networks”, Prentice Hall

COMPUTER VISION
(Professional Elective-1)

I-M. Tech I Semester **L T P C**
Course Code: B1ES103PE **3 0 0 3**

COURSE OBJECTIVES:

1. To introduce students the fundamentals of image formation, major ideas, methods, and techniques of computer vision and pattern recognition;
2. To develop an appreciation for various issues in the design of computer vision and object recognition systems
3. To provide the student with programming experience from implementing computer vision and object recognition application

COURSE OUTCOMES: At the end of this course, students will be able to

1. Study the image formation models and feature extraction for computer vision
2. Identify the segmentation and motion detection and estimation techniques
3. Develop small applications and detect the objects in various applications

UNIT – I

Image Formation Models Monocular imaging system • Orthographic & Perspective Projection • Camera model and Camera calibration • Binocular imaging systems, Perspective, Binocular Stereopsis: Camera and Epipolar Geometry; Homography, Rectification, DLT, RANSAC, 3-D reconstruction framework; Auto-calibration. Apparel, Binocular Stereopsis: Camera and Epipolar Geometry; Homography, Rectification, DLT, RANSAC, 3-D reconstruction framework; Auto- calibration. Apparel, Stereo vision

UNIT – II

Feature Extraction: Image representations (continuous and discrete) • Edge detection, Edge linking, corner detection, texture, binary shape analysis, boundary pattern analysis, circle and ellipse detection, Light at Surfaces; Phong Model; Reflectance Map; Albedo estimation; Photometric Stereo; Use of Surface Smoothness Constraint; Shape from Texture, color, motion and edges.

UNIT – III

Shape Representation and Segmentation: Deformable curves and surfaces • Snakes and active contours Level set representations • Fourier and wavelet descriptors • Medial representations • Multi-resolution analysis, Region Growing, Edge Based approaches to segmentation, Graph-Cut, Mean- Shift, MRFs, Texture Segmentation

UNIT – IV

Motion Detection and Estimation • Regularization theory • Optical computation • Stereo Vision Motion estimation, Background Subtraction and Modelling, Optical Flow, KLT, Spatio- Temporal Analysis, Dynamic Stereo; Motion parameter estimation • Structure from motion, Motion Tracking inVideo

UNIT – V

Object recognition • Hough transforms and other simple object recognition methods • Shape correspondence and shape matching • Principal component analysis • Shape priors for recognition

TEXT BOOKS:

1. D. Forsyth and J. Ponce, "Computer Vision - A modern approach", 2nd Edition, PearsonPrentice Hall, 2012
2. Szeliski, Richard, "Computer Vision: Algorithms and Applications", 1st Edition, Springer-Verlag London Limited, 2011.
3. Richard Hartley and Andrew Zisserman, "Multiple View Geometry in Computer Vision", 2ndEdition, Cambridge University Press, 2004.

REFERENCE BOOKS:

1. K.Fukunaga, "Introduction to Statistical Pattern Recognition", 2nd Edition,Morgan Kaufmann 1990.
2. Rafael C. Gonzalez and Richard E. Woods," Digital Image Processing", 3rd Edition,Prentice Hall, 2008.
3. B. K. P. Horn, "Robot Vision", 1st Edition, McGraw-Hill, 1986.
4. E. R. Davies "Computer and Machine Vision: Theory, Algorithms, Practicalities", 4th Edition,Elsevier Inc, 2012.

COMMUNICATION BUSES AND INTERFACES
(Professional Elective - II)

I-M. Tech I Semester | **L T P C**
Course Code: B1ES104PE | **3 0 0 3**

COURSE OBJECTIVES:
1. To introduce various serial inter falls and design applications.
2. To introduce CAN and PCI protocols.
3. To introduce developing of API for data transfer on serial bus.
4. To teach students design and development of peripherals to do data transfer

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT – I
Serial Busses - Physical interface, Data and Control signals, features, limitations and applications ofRS232, RS485, I^2C, SPI

UNIT – II
CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT – III
PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT – IV
USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT – V
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiberoptic and copper cable

TEXT BOOKS:
1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems”, Lakeview Research, 2nd Edition
2. Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press

REFERENCE BOOKS:
1. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
2. Serial Front Panel Draft Standard VITA 17.1 – 200x
3. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

PARALLEL PROCESSING
(Professional Elective - II)

I-M. Tech I Semester **L T P C**
Course Code: B1ES105PE **3 0 0 3**

COURSE OBJECTIVES:

1. To learn the concept of parallel processing and implementation of pipelining.
2. To introduce upcoming VLIW processor with case study of protocol applications.
3. To introduce multithreaded architecture and discuss various issues & performance protocols.
4. To familiarize with operating systems for multiprocessor system

COURSE OUTCOMES: At the end of this course, students will be able to

1. Identify limitations of different architectures of computer
2. Analysis quantitatively the performance parameters for different architectures
3. Investigate issues related to compilers and instruction set based on type of architectures.

UNIT – I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability, Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT – II

VLIW processors: Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT – III

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT – IV

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

UNIT –V

Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

TEXT BOOKS:

1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGHInternational Edition
2. Kai Hwang, “Advanced Computer Architecture”, TMH

REFERENCE BOOKS:

1. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.
2. William Stallings, “Computer Organization and Architecture, Designing for performance”Prentice Hall, Sixth edition
3. Kai Hwang, Zhiwei Xu, “Scalable Parallel Computing”, MGH
4. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, MorganKaufmann.

ADVANCED COMPUTER ARCHITECTURE
(Professional Elective – II)

I-M. Tech I Semester **L T P C**
Course Code: B1ES106PE **3 0 0 3**

COURSE OBJECTIVES:

1. To make students know about the Parallelism concepts in Programming
2. To give the students an elaborate idea about the different memory systems and buses.
3. To introduce the advanced processor architectures to the students

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand pipelining, instruction set architectures, memory addressing.
2. Understand multithreading by using ILP and supporting thread-level parallelism (TLP).
3. Solve Practical issues in interconnecting networks

UNIT – I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT – III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rdEdition, Elsevier.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A DesignSpace Approach", Pearson Education

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, “Modern Processor Design: Fundamentals of SuperScalar Processors”, 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., “Computer Architecture and Parallel Processing”, Mc Graw Hill.

SYSTEM DESIGN WITH EMBEDDED LINUX LAB

I-M. Tech I Semester **L T P C**
Course Code: B1ES104PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. To understand and make effective use of Linux utilities and Shell scripting language (bash) to solve Problems.
2. To implement in C some standard Linux utilities such as ls, mv, cp etc. using system calls.
3. To develop the skills necessary for systems programming including file system programming, process and signal management, and interprocess communication.

COURSE OUTCOMES: At the end of the laboratory work, students will be able to:

1. Demonstrate the flashing OS onto the devices
2. Develop and interface the different devices like Arduino, Raspbery Pi, Beaglebone
3. Appreciate the necessity of Inter Process Communication and synchronization mechanisms
4. Apply the concept of hosting the website on board and interfacing the USB webcam

LIST OF EXPERIMENTS:

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surroundinglight intensity & automatically turn ON/OFF the high intensity LED's by taking some pre- defined threshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website (static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB

I-M. Tech I Semester **L T P C**
Course Code: B1ES105PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. To Implement the Applications & Programming model of ARM Cortex-M3 processor
2. To implement Priority, Vector Tables, LPC 17xx microcontroller etc.
3. To learn about DSP (P-DSP) Processors, VLIW architecture and TMS320C6000 series

COURSE OUTCOMES: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processorcore SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on theCortex M3 and DSP development boards.

LIST OF ASSIGNMENTS:

Part A)

Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED onceevery five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B)

Experiments to be carried out on DSP C6713 evaluation kits and using Code ComposerStudio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any twopoints
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

ENGLISH FOR RESEARCH PAPER WRITING
(Audit Course - I)

I-M. Tech I Semester **L T P C**
Course Code: B1ES101AC **2 0 0 0**

COURSE OBJECTIVES:

1. To improve student writing skills and level of readability
2. To Learn about what to write in each section
3. To develop the student writing skills

COURSE OUTCOMES: At the end of the course students will be able to:

1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title Ensure the good quality of paper at veryfirst-time submission

UNIT – I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT – II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT – III

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT – IV

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT – V

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOK:

1. Adrian Wallwork, English for Writing Research Papers, Springer New York DordrechtHeidelberg London, 2011

REFERENCES BOOKS

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.

RESEARCH METHODOLOGY AND IPR
(Audit Course – I)

I-M. Tech I Semester **L T P C**
Course Code: B1ES102AC **2 0 0 0**

COURSE OBJECTIVES: The course should enable the students to:

1. Identify an appropriate research problem in their interesting domain.
2. Understand ethical issues understand the Preparation of a research project thesis report.
3. Understand the Preparation of a research project thesis report
4. Understand the law of patent and copyrights & Adequate knowledge on

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by Computer, Information Technology, buttomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Rightto be promoted among students in general & engineering in particular.
6. Understand that IPR protection provides an incentive to inventors for further research workand investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT – I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a goodresearch problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation,Necessary instrumentations

UNIT – II

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT – III

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format ofresearch proposal, a presentation and assessment by a review committee

UNIT – IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT – V

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd, 2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in NewTechnological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

I-YEAR (II-SEMESTER)

RTL SIMULATION AND SYNTHESIS WITH PLDs

I-M. Tech II Semester **L T P C**
Course Code: B1ES201PC **3 0 0 3**

COURSE OBJECTIVES:

1. To learn the basis of RTL programming.
2. To learn the design entry by verilog & VHDL.
3. To learn the basis of ASIC, FPGA and SOC

COURSE OUTCOMES: At the end of the course, students will demonstrate the ability to:

1. Familiarity of Finite State Machines, RTL design using reconfigurable logic.
2. Design and develop IP cores and Prototypes with performance guarantees
3. Use EDA tools like Cadence, Mentor Graphics and Xilinx

UNIT – I

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

UNIT – II

Design entry by Verilog/VHDL/FSM, Verilog AMS.

UNIT – III

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

UNIT – IV

Design for performance, Low power VLSI design techniques. Design for testability.

UNIT – V

IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist,Physical IP, Use of external hard IP during prototyping

TEXT BOOKS:

1. Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
2. Donald D Givone, “Digital principles and Design”, TMH
3. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books.

REFERENCE BOOKS:

1. Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
2. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
3. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodologymanual”, Xilinx

ADVANCED DIGITAL SIGNAL PROCESSING

I-M. Tech II Semester **L T P C**
Course Code: B1ES202PC **3 0 0 3**

COURSE OBJECTIVES:

1. To Comprehend characteristics of discrete time signals and systems
2. To analyze and process signals using various transform techniques
3. To identify various factors involved in design of digital filters
4. To illustrate the effects of finite word length implementation

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand theory of different filters and algorithms
2. Understand theory of multirate DSP, solve numerical problems and write algorithms
3. Understand theory of prediction and solution of normal equations
4. Know applications of DSP at block level.

UNIT – I

Overview of DSP, Characterization in time and frequency, FFT Algorithms, Digital filter design and structures: Basic FIR/IIR filter design &structures, design techniques of linear phase FIR filters, IIR filters by impulse invariance, bilinear transformation, FIR/IIR Cascaded lattice structures, parallel realization of IIR.

UNIT – II

Multi rate DSP, Decimators and Interpolators, Sampling rate conversion, multistage decimator & interpolator, poly phase filters, QMF, digital filter banks, Applications in subband coding.

UNIT – III

Linear prediction & optimum linear filters, stationary random process, forward-backward linear prediction filters, solution of normal equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.

UNIT – IV

Adaptive Filters, Applications, Gradient Adaptive Lattice, Minimum mean square criterion, LMS algorithm, Recursive Least Square algorithm

UNIT – V

Estimation of Spectra from Finite-Duration Observations of Signals. Nonparametric Methods for Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation, Minimum- Variance Spectral Estimation, Eigen analysis Algorithms for Spectrum Estimation.

TEXT BOOKS:

1. J. G. Proakis and D.G. Manolakis, “Digital signal processing: Principles, Algorithm and Applications”, 4th Edition, Prentice Hall, 2007.
2. N. J. Fliege, “Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets”, 1st Edition, John Wiley and Sons Ltd, 1999.
3. D. G. Manolakis, V. K. Ingle and S. M. Kogon, “Statistical and Adaptive Signal Processing”,McGraw Hill, 2000

REFERENCE BOOKS:

1. Bruce W. Suter, “Multirate and Wavelet Signal Processing”,1st Edition, Academic Press,1997.
2. M. H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley & Sons Inc.,2002.
3. S. Haykin, “Adaptive Filter Theory”, 4th Edition, Prentice Hall, 2001.

EMBEDDED COMPUTING

I-M. Tech II Semester **L T P C**
Course Code: B1ES203PC **3 0 0 3**

COURSE OBJECTIVES:

1. To understand the significance of embedded Linux Platform in real time applications.
2. To Know different types of communication protocols like serial and parallel communication protocols
3. To understand wired Interfacing Modules
4. To understand and gain knowledge on wireless sensors and its application in wireless embedded networks

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand the operating system and programming on Linux
2. Implement the software development tools like gdb,lint etc
3. Learn the interfacing of different modules and to handle the interrupt
4. Solve problems using assembler directives, simulation and debugging tools.

UNIT – I

Programming on Linux Platform: System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box
Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT – II

Introduction to Software Development Tools: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,

UNIT – III

Interfacing Modules: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, Open CV for machine vision, Audio signal processing.

UNIT – IV

Networking Basics: Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT – V

IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency,assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:

1. Peter Barry and Patrick Crowley, "Modern Embedded Computing",1st Edition.,Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:

1. Abraham Silberschatz, Peter B. Galvin and Greg Gagne, "Operating System Concepts", Wiley
2. Maurice J. Bach, "The Design of the UNIX Operating System", Prentice-Hall
3. W. Richard Stevens, "UNIX Network Programming", Pearson

IOT AND ITS APPLICATIONS
(Professional Elective – III)

I-M. Tech II Semester **L T P C**
Course Code: B1ES207PE **3 0 0 3**

COURSE OBJECTIVES:
1. To learn IOT technology, security, standardization.
2. To learn IOT radiation, design principle.
3. To learn about private implementation security issues in platform and design IOT application for industrial use.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Understand the concept of IOT and M2M
2. Study IOT architecture and applications in various fields
3. Study the security and privacy issues in IOT.

UNIT – I
IoT& Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT RelatedStandardization, Recommendations on Research Topics.

UNIT – II
M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value
chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT – III
IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

UNIT – IV
IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

UNIT – V
Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues,

TEXT BOOKS:
1. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014.
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to ConnectingEverything", 1st Edition, Apress Publications, 2013.

REFERENCE BOOKS:
1. Cuno Pfister, "Getting Started with the Internet of Things", O Reilly Media, 2011.

VLSI SIGNAL PROCESSING
(Professional Elective - III)

I-M. Tech II Semester **L T P C**
Course Code: B1ES208PE **3 0 0 3**

COURSE OBJECTIVES:
1. To give knowledge about DSP algorithm.
2. To explain about retiming techniques, folding and register minimization path problem.
3. To introduce abut algorithm strength reduction techniques & parallel processing of FIR and IIR filters.
4. To explain about finite word length effects and round off noise computation in DSP.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Ability to modify the existing or new DSP architectures suitable for VLSI.
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Ability to implement fast convolution algorithms.
4. Low power design aspects of processors for signal processing and wireless applications.

UNIT – I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSPalgorithms
Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power
Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, RetimingTechniques

UNIT – II
Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimizationTechniques, Register minimization in folded architectures, folding of Multirate systems
Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT – III
Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT – IV
Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT – V
Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches
Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS:
1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, Wiley Inter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall,1985.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing –Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing – Medisetti V. K, IEEE Press (NY), 1995.

SOC ARCHITECTURE
(Professional Elective - III)

I-M. Tech II Semester **L T P C**
Course Code: B1ES209PE **3 0 0 3**

COURSE OBJECTIVES:
1. To familiarize the basis of SOC design and its architectural issues.
2. To familiarize the design flow and verification of ASIP's and NISC's along with various design methodologies.
3. To introduce the functional simulation, synthesis, layout and timing analysis of single and multi-core systems.
4. To adapt the concept of voltage scaling & optimization of various design parameters oon the basis of case studies.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Understand the components of system, hardware and software.
2. Know the basic concepts of processor architecture and instructions.
3. Describe external and internal memory of SOC.
4. Get knowledge of bus models of SOC 3.

UNIT – I
Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II
Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III
Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT – IV
Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V
Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:
1. Michael J. Flynn and Wayne Luk, "Computer System Design System-on-Chip", Wiley IndiaPvt. Ltd.
2. Steve Furber, "ARM System on Chip Architecture ", 2nd Edition, 2000, Addison WesleyProfessional.

REFERENCE BOOKS:

1. Ricardo Reis, “”Design of System on a Chip: Devices and Components”, 1st Edition, 2004,Springer
2. Jason Andrews, “Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)”, Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, “System on Chip Verification –Methodologies and Techniques”, 2001, Kluwer Academic Publishers.

ARTIFICIAL NEURAL NETWORKS
(Professional Elective - IV)

I-M. Tech II Semester **L T P C**
Course Code: B1ES210PE **3 0 0 3**

COURSE OBJECTIVES:

1. To Survey of attractive applications of Artificial Neural Networks.
2. To practical approach for using Artificial Neural Networks in various technical, organizational and economic applications
3. To understand Associative Memories

COURSE OUTCOMES: At the end of the course, students will be able to:

1. To understand artificial neural network models and their training algorithms
2. To understand the concept of fuzzy logic system components, fuzzification and defuzzification
3. Applies the above concepts to real-world problems and applications.

UNIT – I

Introduction to Neural Networks: Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Hodgkin-Huxley Neuron Model, Integrateand-Fire Neuron Model, Spiking Neuron Model, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN.

Essentials of Artificial Neural Networks: Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Types of Application.

UNIT – II

Feed Forward Neural Networks: Single Layer Feed Forward Neural Networks: Introduction,

Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications.

Multilayer Feed forward Neural Networks: Credit Assignment Problem, Generalized Delta Rule, Derivation of Backpropagation (BP) Training, Summary of Backpropagation Algorithm, Kolmogorov Theorem, Learning Difficulties and Improvements.

UNIT – III

Associative Memories: Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory (Associative Matrix, Association Rules, Hamming Distance, The Linear Associator, Matrix Memories, Content Addressable Memory). Bidirectional Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM Stability Theorem. Architecture of Hopfield Network: Discrete and Continuous versions, Storage and Recall Algorithm, Stability Analysis, Capacity of the Hopfield Network.

UNIT –IV

Classical and Fuzzy Sets: Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions.

UNIT – V

Fuzzy Logic System: Fuzzification, Membership value assignment, development of rule base and decision-making system, Defuzzification to crisp sets, Defuzzification methods.

TEXT BOOKS:

1. Rajasekharan and Pai, Neural Networks, Fuzzy logic, Genetic algorithms: synthesis and applications– PHI Publication.
2. Satish Kumar, Neural Networks, TMH, 2004.

REFERENCE BOOKS:

1. James A Freeman and Davis Skapura, Neural Networks, Pearson Education, 2002.
2. Simon Hakins, Neural Networks, Pearson Education.
3. C. Eliasmith and Ch. Anderson, Neural Engineering, PHI.

NETWORK SECURITY AND CRYPTOGRAPHY
(Professional Elective - IV)

I-M. Tech II Semester **L T P C**
Course Code: B1ES211PE **3 0 0 3**

COURSE OBJECTIVES:

1. To introduce basic and advanced concepts of security.
2. To introduce various cryptography techniques.
3. To teach students various authentication techniques and to introduce various threats.

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT – I

Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Modelfor Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT – II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT – III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT – IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT – V

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", PearsonEducation, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, PrivateCommunication in a Public World", Prentice Hall, 2nd Edition

REFERENCE BOOKS:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, DesignDeployment and Operations", RSA Pres,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "InsideNetwork Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding IncidentDetection and Response", William Pollock Publisher, 2013.

PHYSICAL DESIGN AUTOMATION
(Professional Elective – IV)

I-M. Tech II Semester L T P C
Course Code: B1ES212PE 3 0 0 3

COURSE OBJECTIVES:
1. To introduce the physical design issues for VLSI automation.
2. To familiarize performance issues of VLSI circuits, various delay models & its estimation.
3. To introduce the placement & routing algorithms.

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Study automation process for VLSI System design.
2. Understanding of fundamentals for various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physicaldesign process of VLSI systems.

UNIT – I
Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT – II
Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT – III
Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT – IV
Global routing: Problem formulation, classification of global routing, Maze routing algorithms, Line- Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.
Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi- Layer channel routing, Algorithms, Switch box routing.

UNIT – V
Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.
Via Minimization: Constraint and Unconstrained via minimization.
Clock and Power Routing: Clocking schemes, design considerations for the clock ,Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS:
1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley& Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:
1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson EducationAsia

ADVANCED DIGITAL SIGNAL PROCESSING LAB

I-M. Tech II Semester **L T P C**
Course Code: B1ES204PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. To perform basic Operations on Signals & program
2. To estimate PSD, Power Spectrum of signals.
3. To study Finite Length Effects using Simulink & ECG signal compression

COURSE OUTCOMES: At the end of the laboratory work, students will be able to:

1. Generates the various signals and its FFT
2. Design and simulate the different filters based on required applications
3. Implement the ECG signal compression and design and simulation of filter

LIST OF EXPERIMENTS:

1. Basic Operations on Signals, Generation of Various Signals and finding its FFT.
2. Program to verify Decimation and Interpolation of a given Sequences.
3. Program to Convert CD data into DVD data
4. Generation of DuTone Multiple Frequency (DTMF) Signals
5. Plot the Periodogram of a Noisy Signal and estimate PSD using Periodogram and ModifiedPeriodogram methods
6. Estimation of Power Spectrum using Bartlett and Welch methods
7. Verification of Autocorrelation Theorem
8. Parametric methods (Yule-Walker and Burg) of Power Spectrum Estimation
9. Estimation of data series using Nth order Forward Predictor and comparing to the Original Signal
10. Design of LPC filter using Levinson-Durbin Algorithm
11. Computation of Reflection Coefficients using Schur Algorithm
12. To study Finite Length Effects using Simulink
13. ECG signal compression
14. Design and Simulation of Notch Filter to remove 60 Hz Hum/any unwanted frequency componentof given Signal (Speech/ECG)

RTL SIMULATION AND SYNTHESIS WITH PLDS LAB

I-M. Tech II Semester **L T P C**
Course Code: B1ES205PC **0 0 3 1.5**

COURSE OBJECTIVES:

1. To learn the basis of RTL programming.
2. To learn the design entry by verilog & VHDL.
3. To learn the basis of ASIC, FPGA and SOC

COURSE OUTCOMES:

At the end of the laboratory work, students will be able to:

1. Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
2. Use EDA tools like Cadence, Mentor Graphics and Xilinx or equivalent tools
3. Implement verilog on arithmetic , DFT and FFT

LIST OF EXPERIMENTS:

1. Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3. Vending machines - Traffic Light controller, ATM, elevator control.
4. PCI Bus & arbiter and downloading on FPGA.
5. UART/ USART implementation in Verilog.
6. Realization of single port SRAM in Verilog.
7. Verilog implementation of Arithmetic circuits like serial adder/ subtractor, paralleladder/subtractor, serial/parallel multiplier.
8. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

DISASTER MANAGMENT
(Audit Course - II)

I-M. Tech II Semester L T P C
Course Code: B1ES203AC 2 0 0 0

COURSE OBJECTIVES:

1. To provide basic conceptual understanding of disasters and its relationships with development.
2. To gain understand approaches of Disaster Risk Reduction (DRR)
3. To maintain the relationship between vulnerability, disasters, disaster prevention and risk reduction.

COURSE OBJECTIVES: Students will be able to

1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice frommultiple perspectives.
3. Develop an understanding of standards of humanitarian response and practical relevance inspecific types of disasters and conflict situations.
4. Critically understand the strengths and weaknesses of disaster management approaches,
5. Planning and programming in different countries, particularly their home country or the countriesthey work in

UNIT – I

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT – II

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT – III

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT – IV

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT –V

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.

REFERENCE BOOKS:

1. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course - II)

I-M. Tech II Semester | **L T P C**
Course Code: B1ES204AC | **2 0 0 0**

PREREQUISITE: None

COURSE OBJECTIVES:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

COURSE OUTCOMES: Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

II-YEAR (I-SEMESTER)

SCRIPTING LANGUAGES
(Professional Elective – V)

II-M. Tech I Semester **L T P C**
Course Code: B1ES313PE **3 0 0 3**

COURSE OBJECTIVES:

1. To explain the characteristics and uses of scripting languages.
2. To describe the various PERL concepts used in VLSI design.
3. To learn the concepts of TCL.
4. To Interpret JavaScript, Python language, Python web system Design

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Understand the differences between typical scripting languages and typical system
2. Gain knowledge of the strengths and weakness of Perl, TCL ,OOPS
3. Select an appropriate language for solving a given problem.
4. Acquire programming skills in scripting language

UNIT – I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built- in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT – II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT – III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT – IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts- and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT – V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes,Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. David Barron, “The World of Scripting Languages”, Wiley Student Edition, 2010.
2. Brent Welch, Ken Jones and Jeff Hobbs., “Practical Programming in Tcl and Tk”– 4th Edition, Prentice Hall
3. Herbert Schildt, “Java the Complete Reference”, 7th Edition, TMH.

REFERENCE BOOKS:

1. Clif Flynt, “Tcl/Tk: A Developer's Guide”, 2003, Morgan Kaufmann Series.
2. John Ousterhout, “Tcl and the Tk Toolkit”, 2nd Edition, 2009, Kindel Edition.
3. Wojciech Kocjan and Piotr Beltowski, “Tcl 8.5 Network Programming book”, PacktPublishing.
4. Bert Wheeler, “Tcl/Tk 8.5 Programming Cookbook”, 2011, Packt PublishingLimited.

MEMORY TECHNOLOGIES
(Professional Elective – V)

II-M. Tech I Semester **L T P C**
Course Code: B1ES314PE **3 0 0 3**

COURSE OBJECTIVES:

1. To introduce about various type of memory Architectures.
2. To introduce about various performance parameter of memory Architectures.
3. To introduce about various memory packing technologies.
4. To introduce about various 2D & 3D memory Architectures

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and theirtesting procedures.
3. Know, how of the state-of-the-art memory chip design

UNIT – I

Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT – II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT – III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT – IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

UNIT – V

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXT BOOKS:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs andApplications”, Wiley Interscience
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition

REFERENCE BOOK:

1. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

WIRELESS SENSOR NETWORKS
(Professional Elective – V)

II-M. Tech I Semester **L T P C**
Course Code: B1ES315PE **3 0 0 3**

COURSE OBJECTIVES:

1. To build understanding of the fundamental concepts of wireless communications and networks.
2. To learn mathematical modeling of a wireless communication channel.
3. To build basic concepts in designing transmitter and receiver of a wireless communication system.
4. To learn different wireless communication network standards.

COURSE OUTCOMES: Upon completion of the course, the student will be able to:

1. Analyze and compare various architectures of Wireless Sensor Networks
2. Understand Design issues and challenges in wireless sensor networks
3. Analyze and compare various data gathering and data dissemination methods.
4. Design, Simulate and Compare the performance of various routing and MAC protocol

UNIT – I

Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT – II

Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT – III

Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol,IEEE 802.15.4 standard and ZigBee

UNIT – IV

Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT – V

Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:

1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE
3. Wireless Communication and Networking – William Stallings, 2003, PHI.

REFERENCE BOOKS:

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

ARTIFICIAL NEURAL NETWORKS
(Open Elective)

II-M. Tech I Semester **L T P C**
Course Code: B1ES301OE **3 0 0 3**

COURSE OBJECTIVES:

1. To Survey of attractive applications of Artificial Neural Networks.
2. To practical approach for using Artificial Neural Networks in various technical, organizational and economic applications
3. To understand Associative Memories

COURSE OUTCOMES: At the end of the course, students will be able to:

1. To understand artificial neural network models and their training algorithms
2. To understand the concept of fuzzy logic system components, fuzzification and defuzzification
3. Applies the above concepts to real-world problems and applications.

UNIT – I

Introduction to Neural Networks: Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Hodgkin-Huxley Neuron Model, Integrateand-Fire Neuron Model, Spiking Neuron Model, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN.

Essentials of Artificial Neural Networks: Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Types of Application.

UNIT – II

Feed Forward Neural Networks: Single Layer Feed Forward Neural Networks: Introduction,

Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications.

Multilayer Feed forward Neural Networks: Credit Assignment Problem, Generalized Delta Rule, Derivation of Backpropagation (BP) Training, Summary of Backpropagation Algorithm, Kolmogorov Theorem, Learning Difficulties and Improvements.

UNIT – III

Associative Memories: Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory (Associative Matrix, Association Rules, Hamming Distance, The Linear Associator, Matrix Memories, Content Addressable Memory). Bidirectional Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM Stability Theorem. Architecture of Hopfield Network: Discrete and Continuous versions, Storage and Recall Algorithm, Stability Analysis, Capacity of the Hopfield Network.

UNIT –IV

Classical and Fuzzy Sets: Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions.

UNIT – V

Fuzzy Logic System: Fuzzification, Membership value assignment, development of rule base and decision-making system, Defuzzification to crisp sets, Defuzzification methods.

TEXT BOOKS:

3. Rajasekharan and Pai, Neural Networks, Fuzzy logic, Genetic algorithms: synthesis and applications– PHI Publication.
4. Satish Kumar, Neural Networks, TMH, 2004.

REFERENCE BOOKS:

4. James A Freeman and Davis Skapura, Neural Networks, Pearson Education, 2002.
5. Simon Hakins, Neural Networks, Pearson Education.
6. C. Eliasmith and Ch. Anderson, Neural Engineering, PHI.

INTERNET OF THINGS
(Open Elective)

II-M. Tech I Semester **L T P C**
Course Code: B1ES302OE **3 0 0 3**

COURSE OBJECTIVES:
1. To learn IOT technology, security, standardization.
2. To learn IOT radiation, design principle.
3. To learn and design IOT application for industrial use.
4. To learn about private implementation security issues in platform

COURSE OBJECTIVES: At the end of the course, students will be able:
1. To introduce the terminology, technology and its applications
2. To introduce the concept of M2M (machine to machine) with necessary protocols
3. To introduce the Python Scripting Language which is used in many IoT devices
4. To introduce the Raspberry PI platform, that is widely used in IoT applications
5. To introduce the implementation of web based services on IoT devices

UNIT – I
Introduction to Internet of Things –Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT communication models, Iot Communication APIs IoT enabaled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems, IoT Levels and Templates Domain Specific IoTs – Home, City, Environment, Energy, Retail, Logistics, Agriculture, Industry, health and Lifestyle

UNIT – II
IoT and M2M – Software defined networks, network function virtualization, difference between SDN and NFV for IoT Basics of IoT System Management with NETCOZF, YANG- NETCONF, YANG, SNMP NETOPEER

UNIT – III
Introduction to Python - Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages - JSON, XML, HTTPLib, URLLib, SMTPLib

UNIT – IV
IoT Physical Devices and Endpoints - Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, reading input from pins.

UNIT – V
IoT Physical Servers and Cloud Offerings – Introduction to Cloud Storage models and communication APIs Webserver – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API

TEXT BOOKS:
1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547
2. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759

REFERENCE BOOKS:

1. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1st Edition, Apress Publications, 2013.
2. Cuno Pfister, “Getting Started with the Internet of Things”, O_Reilly Media, 2011

AD HOC AND SENSOR NETWORKS
(Open Elective)

II-M. Tech I Semester **L T P C**
Course Code: B1ES303OE **3 0 0 3**

COURSE OBJECTIVES:
1. To understand the different issues in Adhoc wireless network.
2. To analyze the design goals of routing protocol for Ad hoc wireless network.
3. To learn about the different routing and transport layer protocols in ad hoc wireless network.
4. To understand QOS and Energy management in Ad hoc wireless network.

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Student will understand the difference between Adhoc wireless and wireless network.
2. Student will implement MAC Protocol in Adhoc wireless networks.
3. Student will design routing protocol in Adhoc wireless networks.
4. Student will implement QOS and energy management in Adhoc wireless network

UNIT – I INTRODUCTION
Fundamentals of Wireless Communication Technology – The Electromagnetic Spectrum – Radio propagation Mechanisms – Characteristics of the Wireless Channel -mobile ad hoc networks (MANETs) and wireless sensor networks (WSNs): concepts and architectures. Applications of Ad Hoc and Sensor networks, Design Challenges in Ad hoc and Sensor Networks.

UNIT – II MAC PROTOCOLS FOR AD HOC WIRELESS NETWORKS
Issues in designing a MAC Protocol- Classification of MAC Protocols- Contention based protocols-Contention based protocols with Reservation Mechanisms- Contention based protocols with Scheduling Mechanisms – Multi channel MAC-IEEE 802.11

UNIT – III ROUTING PROTOCOLS AND TRANSPORT LAYER IN AD HOC WIRELESS NETWORKS
Issues in designing a routing and Transport Layer protocol for Ad hoc networks- proactive routing, reactive routing (on-demand), hybrid routing- Classification of Transport Layer solutions-TCP over Ad hoc wireless Networks.

UNIT – IV WIRELESS SENSOR NETWORKS (WSNS) AND MAC PROTOCOLS
Single node architecture: hardware and software components of a sensor node – WSN Network architecture: typical network architectures-data relaying and aggregation strategies -MAC layer protocols: self-organizing, Hybrid TDMA/FDMA and CSMA based MAC- IEEE 802.15.4.

UNIT – V WSN ROUTING, LOCALIZATION & QOS
Issues in WSN routing – OLSR- Localization – Indoor and Sensor Network Localization-absolute and relative localization, triangulation-QOS in WSN-Energy Efficient Design-Synchronization-Transport Layer issues

TEXT BOOKS:
1. C. Siva Ram Murthy, and B. S. Manoj, “Ad Hoc Wireless Networks: Architectures and Protocols”, Prentice Hall Professional Technical Reference, 2008.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-Technology, Protocols, and Applications”, John Wiley, 2007
3. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.

REFERENCE BOOKS:

1. Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc & Sensor Networks: Theory and Applications", World Scientific Publishing Company, 2006.
2. Feng Zhao and Leonides Guibas, "Wireless Sensor Networks", Elsevier Publication – 2002.
3. Holger Karl and Andreas Willig "Protocols and Architectures for Wireless Sensor Networks", Wiley, 2005

INFORMATION RETRIEVAL SYSTEMS
(Open Elective)

II M. Tech I Semester **L T P C**
Course Code: B1ES304OE **3 0 0 3**

COURSE OUTCOMES: At the end of the course, students will be able to:

1. Use different information retrieval techniques in various application areas
2. Apply IR principles to locate relevant information large collections of data
3. Analyze performance of retrieval systems when dealing with unmanaged data sources
4. Implement retrieval systems for web search tasks.

UNIT – I
Boolean retrieval. The term vocabulary and postings lists. Dictionaries and tolerant retrieval. Index construction. Index compression

UNIT – II
Scoring, term weighting, and the vector space model. Computing scores in a complete search system. Evaluation in information retrieval Relevance feedback and query expansion

UNIT – III
XML retrieval. Probabilistic information retrieval. Language models for information retrieval. Text classification. Vector space classification

UNIT – IV
Support vector machines and machine learning on documents, Flat clustering, Hierarchical clustering, Matrix decompositions and latent semantic indexing.

UNIT – V
Web search basics. Web crawling and indexes, Link analysis

TEXT BOOKS:
1. Introduction to Information Retrieval , Christopher D. Manning and Prabhakar Raghavan and Hinrich Schütze, Cambridge University Press, 2008.

REFERENCE BOOKS:
1. Information Storage and Retrieval Systems: Theory and Implementation, Kowalski, Gerald, Mark T Maybury, Springer.
2. Modern Information Retrieval, Ricardo Baeza-Yates, Pearson Education, 2007.
3. Information Retrieval: Algorithms and Heuristics, David A Grossman and Ophir Frieder, 2nd Edition, Springer, 2004.
4. Information Retrieval Data Structures and Algorithms, William B Frakes, Ricardo BaezaYates, Pearson Education, 1992.
5. Information Storage & Retieval, Robert Korfhage, John Wiley, & Sons.